TM 11–6625-2610–40

TECHNICAL MANUAL

GENERAL SUPPORT MAINTENANCE MANUAL

RADAR TEST SET AN/TPM-25A
(NSN 6625-01-045-9988)

HEADQUARTERS, DEPARTMENT OF THE ARMY
AUGUST 1979

WARNING

Be careful when working with the 115-volt power connections. SERIOUS INJURY or DEATH may result from contact with these terminals.

CAUTION

This equipment contains highly sophisticated, complicated circuitry. Maintenance personnel should not attempt any maintenance without reading and fully understanding the applicable section relating to that maintenance.

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WASHINGTON, DC *10 AUGUST 1979*

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REPORTING OF ERRORS

You can improve this manual by recommending improvements using DA Form 2028-2 located in the back of the manual. Simply tear out the self-addressed form, fill it out as shown on the sample, fold it where shown, and drop it in the mail.

If there are no blank DA Forms 2028-2 in the back of your manual, use the standard DA Form 2028 (Recommended Changes to Publications and Blank Forms) and forward to the Commander, U.S. Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, NJ 07703.

In either case a reply will be furnished direct to you.

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS — Continued

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1-1. Scope

a. This manual provides general support maintenance instructions for Radar Test Set AN/TPM–25A (test set). It includes a description of the functioning of the equipment, general support maintenance instructions, and diagrams. The maintenance instructions cover troubleshooting, removal and replacement instructions, adjustment and alignment procedures, repair instructions, and testing procedures.

b. Operator and organizational maintenance instructions are contained in TM 11 –6625–2610–12.

1–2. Indexes of Publications

a. DA Pam 310–4. Refer to the latest issue of DA Pam 310–4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. DA Pam 310-7 Refer to the latest issue of DA Pam 310–7 to determine whether there are modification work orders (MWOs) pertaining to the equipment,

1-3. Forms and Records

a. Reports of Maintenance and Unsatisfactory Equipment. Maintenance forms, records, and reports which are to be used by maintenance personnel at all maintenance levels are listed in and prescribed by TM 38–750.

b. Report of Packaging and Handling Deficiencies. Fill out and forward DD Form 6 (Packaging Improvement Report) as prescribed in AR 700–58/ NAVSUPINST 4030.29/AFR 71–13/MCO P4030.29A and DLAR 4145.8.

c. *Discrepancy in Shipment Report (DISREP) (SF 361).* Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55–38/NAVSUPINST 4610.33 B/AFR 75-18/MCO P4610.19C and DLAR 4500.15.

1-4. Reporting Equipment Improvement Recommendations (EIR)

EIR's will be prepared using Standard Form 368, Quality Deficiency Report. Instructions for preparing EIR's are provided in TM 38–750, The Army Maintenance Management System. EIRs should be mailed directly to Commander, US Army Communications and Electronic Materiel Readiness Command, ATTN: DRSEL–ME–MQ, Fort Monmouth, NJ 07703. A reply will be furnished to you.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

Section 1. OVERALL FUNCTIONAL DESCRIPTION

NOTE

Signal names will be given in the text exactly as shown in the schematic diagrams and will not be capitalized.

2-1. Overall Function

Radar Test Set AN/TPM–25A (test set) provides the capabilities for testing, calibrating and maintaining, IFF interrogator systems. The test set generates synchronizing triggers (radar trigger and SIF pretrigger) to initiate interrogator set transmissions (IFF challenges). It demodulates these IFF challenges so they can be analyzed for proper frequency, power level, coding, timing, pulse shape, and pulse spacings by observations and measurements with an oscilloscope. The test set also simulates a transponder by generating rf and video replies to test receiver sensitivities and bandwidths; preselector alignments; interleaved dynamic range characteristics; GTC adjustments, RSLS comparison; SIF decoder; and SIF degarbling characteristics. Gated SIF and mode 4 replies (with synchronized jamming signals) are provided to test target and friend threshold criteria. In addition, a mode 4 challenge video pulse train and GTC trigger are provided to test the receiver-transmitter without the KIR–lA/TSEC computer. SIF challenge video from the test set SIF CHAL VID CHAL VID OUT jack maybe provided directly to the interrogator set receiver-transmitter without the use of the interrogator synchronizer. An input for low power measurements is also available. A self-test feature permits isolation of failures to a printed circuit card and/or module level using only the test set indicators and test points. Test set cable connections are shown on figure 2–1.

Section II. FUNCTIONAL DESCRIPTION

2-2. General

The test set operates in either swept frequency or fixed frequency. Swept frequency is selected by setting the SIG GEN FUNCTION switch to either SWP ±5 MHZ or SWP ±15 MHZ. Swept frequency is selected when measuring interrogator receiver bandwidth characteristics or interrogator transmitter frequency. Fixed frequency is selected by setting the SIG GEN FUNCTION switch to FIXED FREQ and is used when measuring all other interrogator characteristics.

2-3. Fixed Frequency Operation

In fixed frequency operation, interrogation timing may be synchronized to the test set PRT Generator Section, to the decoded challenge input signal PRF from the interrogator under test or to a trigger from a source external to the test set. Replies generated by the test set are triggered and delayed from the test set PRT Generator Section zero (0) trigger, from a decoded challenge input signal, or from a trigger from a source external to the test set. Interrogation triggering and reply signal triggering are selected by the test set TRIG SEL DCD MODE SEL switch and TRIG SEL INT/DCD/EXT switch.

a. Internal Triggering. With the TRIG SEL INT/DCD/EXT switch to INT, the test set generates the following outputs in response to an internally generated PRT trigger: a radar trigger, a scope trigger, SIF challenge video (when enabled by the SIF CHAL VID SIF MODE SEL switch), SIF pretrigger, mode 4 challenge video, and mode 4 GTC trigger. For this test set operation, the radar trigger (RDR TRIG) or SIF pretrigger (SIF CHAL VID PRE TRIG) is used by the interrogator under test to establish the basic system timing. The external oscilloscope sweep is synchronized by the scope trigger (MEASUREMENT SCOPE TRIG) output. The oscilloscope is used to measure the characteristics of the detected challenge signal.

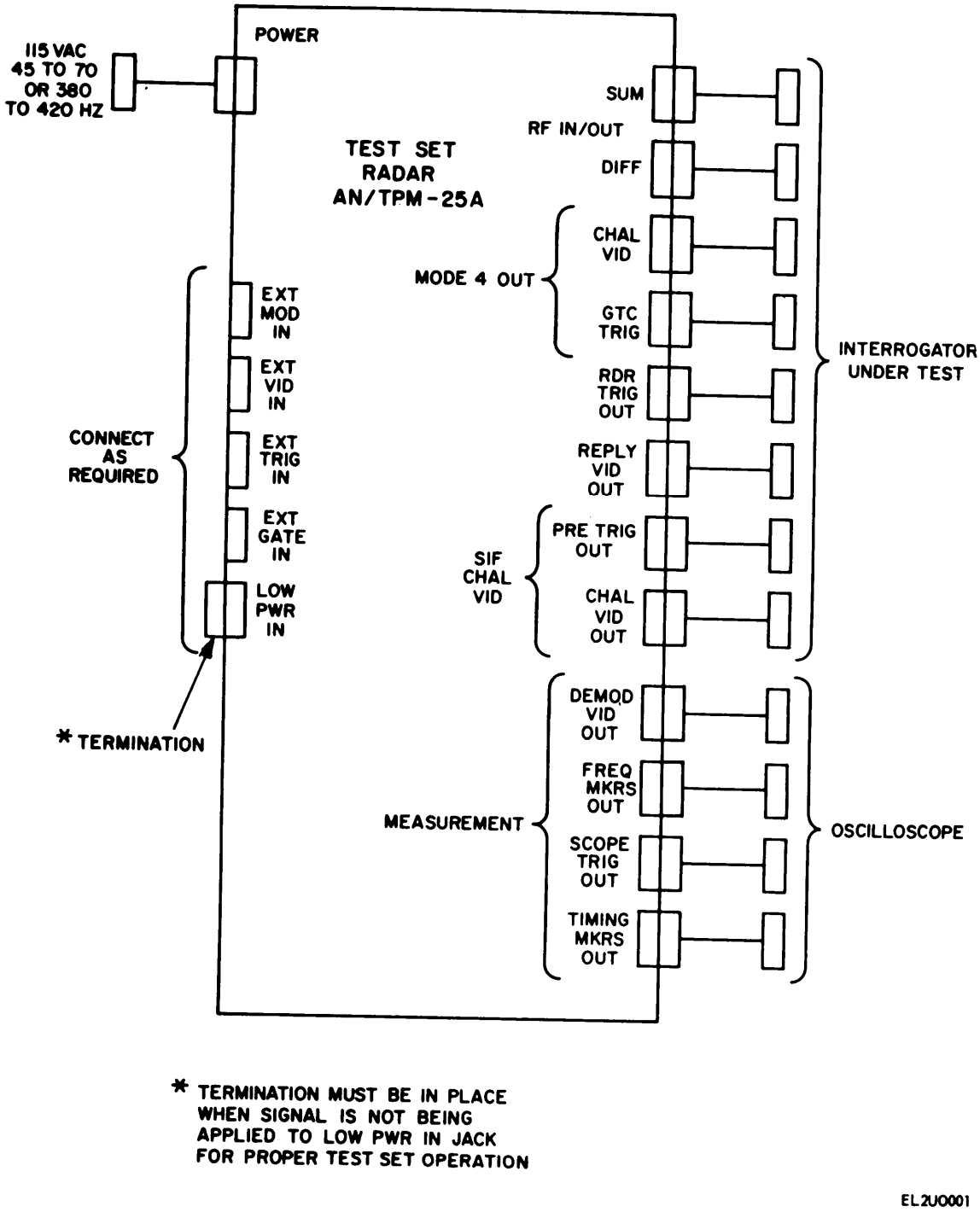

Figure 2-1. Test set input and output connection diagram.

b. DCD Triggering, With the TRIG SEL INT/DCD/EXT switch to DCD, the test set PRT generator is inactive, the test set replies are synchronized to the incoming challenge from the interrogator under test in the following manner. The challenge signal from the interrogator under test is detected and decoded by the test set. If the mode ofinterrogation matches the mode selected by the test set TRIG SEL DCD MODE SEL switch, the test set generates a reply signal to be returned to the interrogator under test. Reply signal generation is described later in this section.

c. External Triggering. With the TRIG SEL INT/DCD/EXT switch in the EXT position, the test

set PRT generator is synchronized to an external trigger input to the TRIG SEL EXT TRIG IN jack. PRT generator operation is the same as internal trigger operation and the test set generates the same outputs as in the internal triggering condition as follows: a radar trigger, a scope trigger, SIF challenge video (when enabled by the SIF CHAL VID SIF MODE SEL switch), SIF pretrigger, mode 4 challenge video, and mode 4 GTC trigger.

d. Reply Code Triggering. With the TRIG SEL DCD MODE SEL switch to a selected mode (any position except OFF) the test set generates a reply in response to a challenge from the interrogator under test when interrogating in the selected mode. SIF replies generated under these conditions are delayed from the interrogations by an amount simulating the transponder turn-around time plus the range delay selected by the REPLIES RANGE DELAY SEL (µSEC) switches. Mode 4 replies generated under these conditions are delayed from the interrogations by a delay simulating the expected mode 4 computer delay (for a more detailed delay description see paragraph 2-3*f*(2)) plus the range delay selected by the REPLIES RANGE DELAY SEL (µSEC) switches. With the TRIG SEL DCD MODE SEL switch in the OFF position, Rf and video replies are synchronized to the internal PRT generator, to the external trigger or are inhibited. With the TRIG SEL INT/DCD EXT switch in the INT position a reply is generated at a PRF established by the internal trigger and delayed. The amount of delay with respect to the radar trigger is established by the test set-preset fixed delays (which simulate interrogator system delays) and range delays (selected by the REPLIES RANGE DELAY SEL (µSEC) switches). In this manner the replies are generated independently of challenges received from the interrogator.

e. *SIF Fixed Frequency Operation.* The simplified block diagram for SIF operation is shown in figure 2-2. SIF fixed frequency trigger timing is shown in figure 2–3.

(1) *SIF challenge pulse generation* (fig. 2–2). The PRT Generator Section produces a 0 trigger signal which is shaped in the Output Trigger Generator Section and then provided as both radar trigger (RDR TRIG) and oscilloscope trigger (SCOPE TRIG) on the front panel of the test set. The PRT Generator Section also provides sif clock and sif gate signals to the Output Trigger Generator Section. The 1 MHZ sif clock signal is used to trigger a shift register in the Output Trigger Generator Section when clocking is enabled by a sif gate signal. Outputs from the shift register are sent to decode gates corresponding to the SIF interrogation pulse positions for P1 and P3 of the enabled SIF interrogation mode. The mode is selected by the SIF CHAL VID SIF MODE switch. The P1 and P3 triggers are shaped and provided as an output signal at SIF CHAL VID CHAL VID OUT jack. The position of the sif gate with respect to rdr trig signal (and therefore the sif chal vid interrogation pulses) is selected by switches S4, S5, and S6 on the Al card. The sif pretrigger signal is also decoded from the shift register and then is shaped and provided as an output signal at the SIF CHAL VID PRE TRIG jack. The position of the sif pretrigger signal with respect to the rdr trig signal is selected by switches S7, S8, and S9 on the Al card.

(2) *Reply pulse generation.* As previously explained, a reply maybe generated as a result of an internal trigger, external trigger, or decoded interrogation from the interrogator under test. In internal trigger or external trigger, a trigger is generated by a decode gate operating from the same clocked shift register that generates the SIF interrogation. This generates a signal that is delayed in the Delay Generator Section by an amount of time selected by the REPLIES RANGE DELAY SEL (pSEC) switch. The minimum dealy between the 0 trigger and reply trigger (normally 434.0 µsec) is set so that the decoded and processed reply is referenced to radar zero range for the type of interrogator under test. The minimum delay occurs when the REPLIES RANGE DELAY SEL (KSEC) switches are set to 0001. The delayed output is provided as a delayed reply trig output to the Reply Video Generator Section. The same action takes place when an interrogation is decoded, except the Delay Generator Section is triggered by a decode trigger signal. The Delay Generator Section also provides the pass/inhibit gating to set up a ratio function allowing replies to be generated to some interrogations and inhibited for others. The 0 trigger pulses, which occur once per interrogation, are counted by a gating counter. A blanking and replies off signal enables replies until a count is reached which corresponds to the number selected by the REPLIES GATING PASS switches. The blanking and replies off signal then inhibits replies until a count is reached which corresponds to the number selected by the REPLIES GATING INHIB switches. If a PASS number of 75 and an INHIB number of 25 were selected, 75 replies would be allowed to occur at a rate of one for each interrogation, then 25 would be allowed to pass with no reply generation after which 75 more replies would be enabled. Gating occurs on the A9 card where reply pulse width one-shots are alternate y enabled or inhibited. Upon receipt of a delayed reply trig signal, the Reply Video Generator Section generates the SIF reply signal to the REPLY VID OUT jack and as sum mod and cliff mod signals to the Rf Generator Section. The SIF reply code is selected by the REPLIES SIF REPLY CODE switches. Pulse width is selected by the REPLIES REPLY WIDTH SELECT and VARY controls. The REPLIES MODULATION SEL switch allows selec-

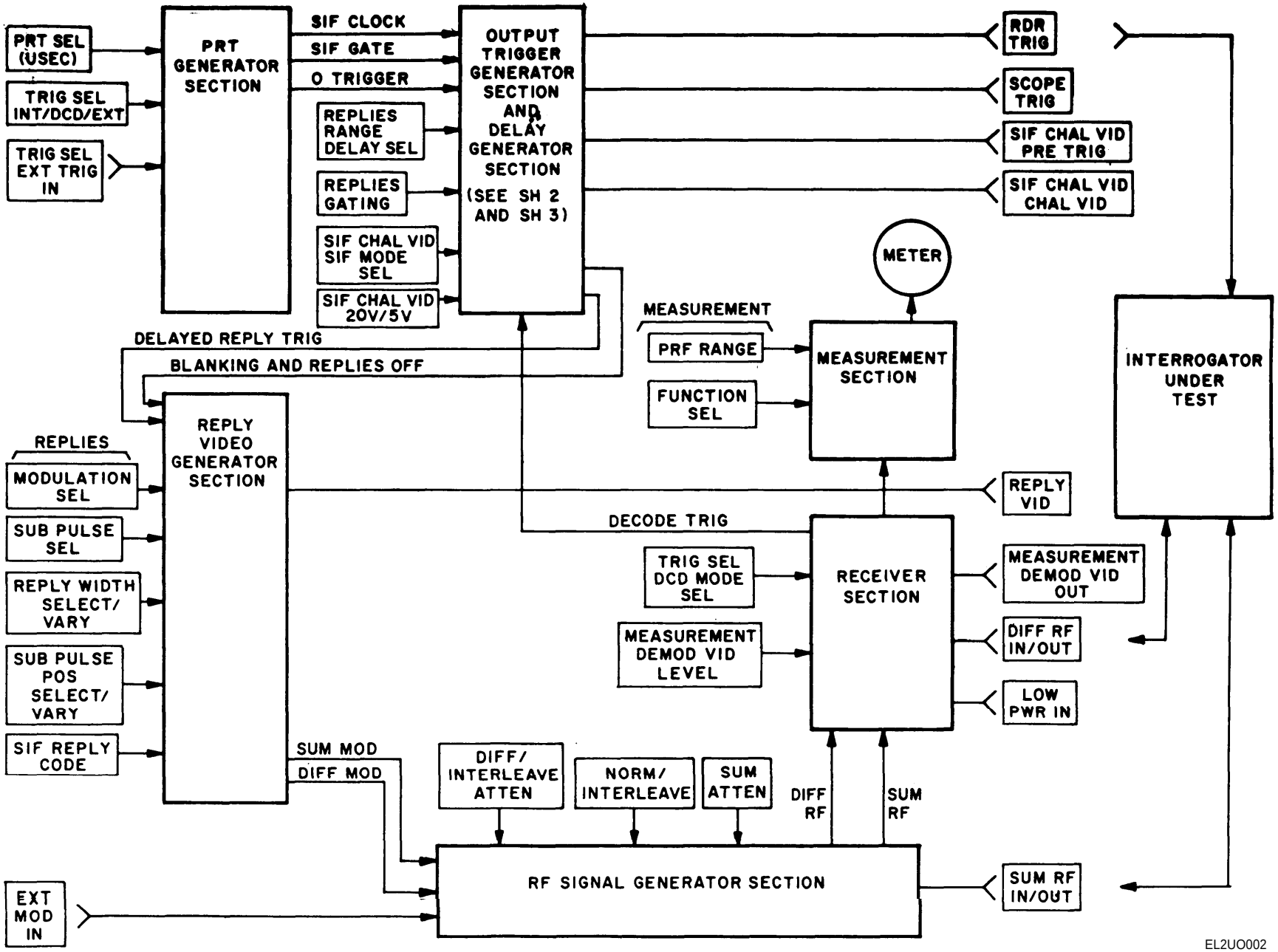

Figure 2-2. SIF fixed frequenqy, simplified block diagram (sheet 1 of 3).

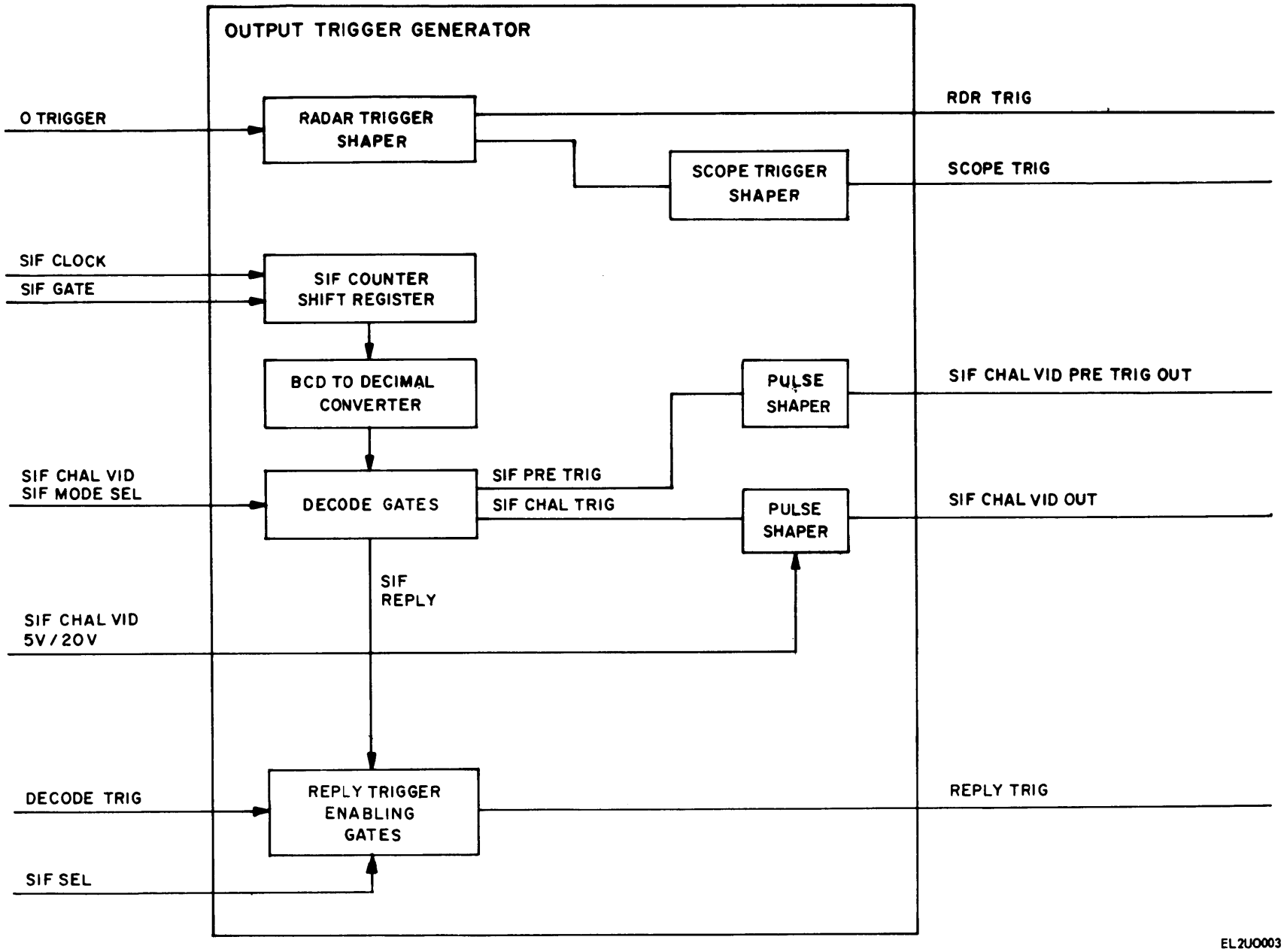

Figure 2–2. SIF fixed frequency, simplified block diagram (sheet 2 of 3).

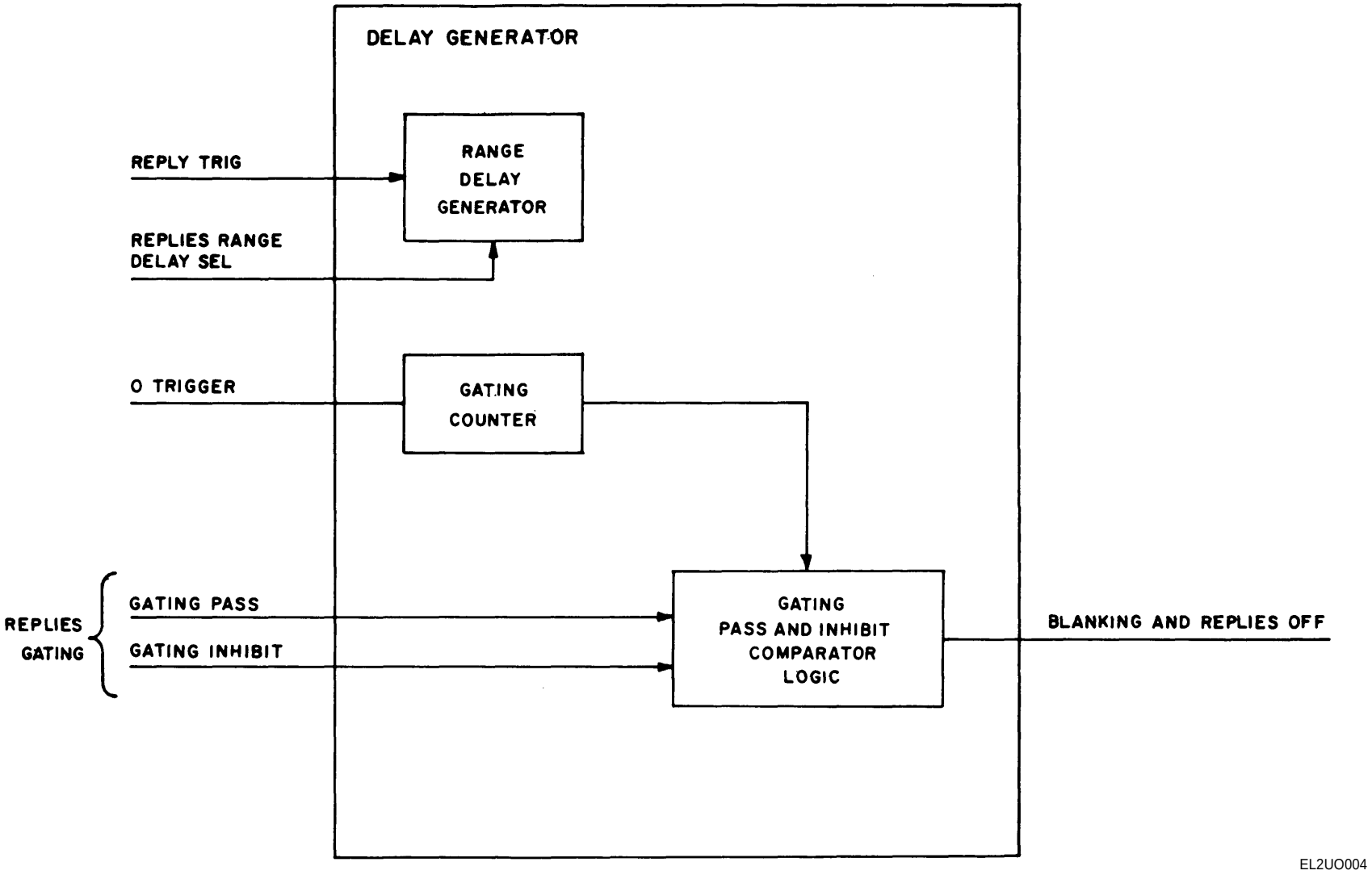

Figure 2-2. SIF fixed frequency, simplified block diagram (sheet 3 of 3).

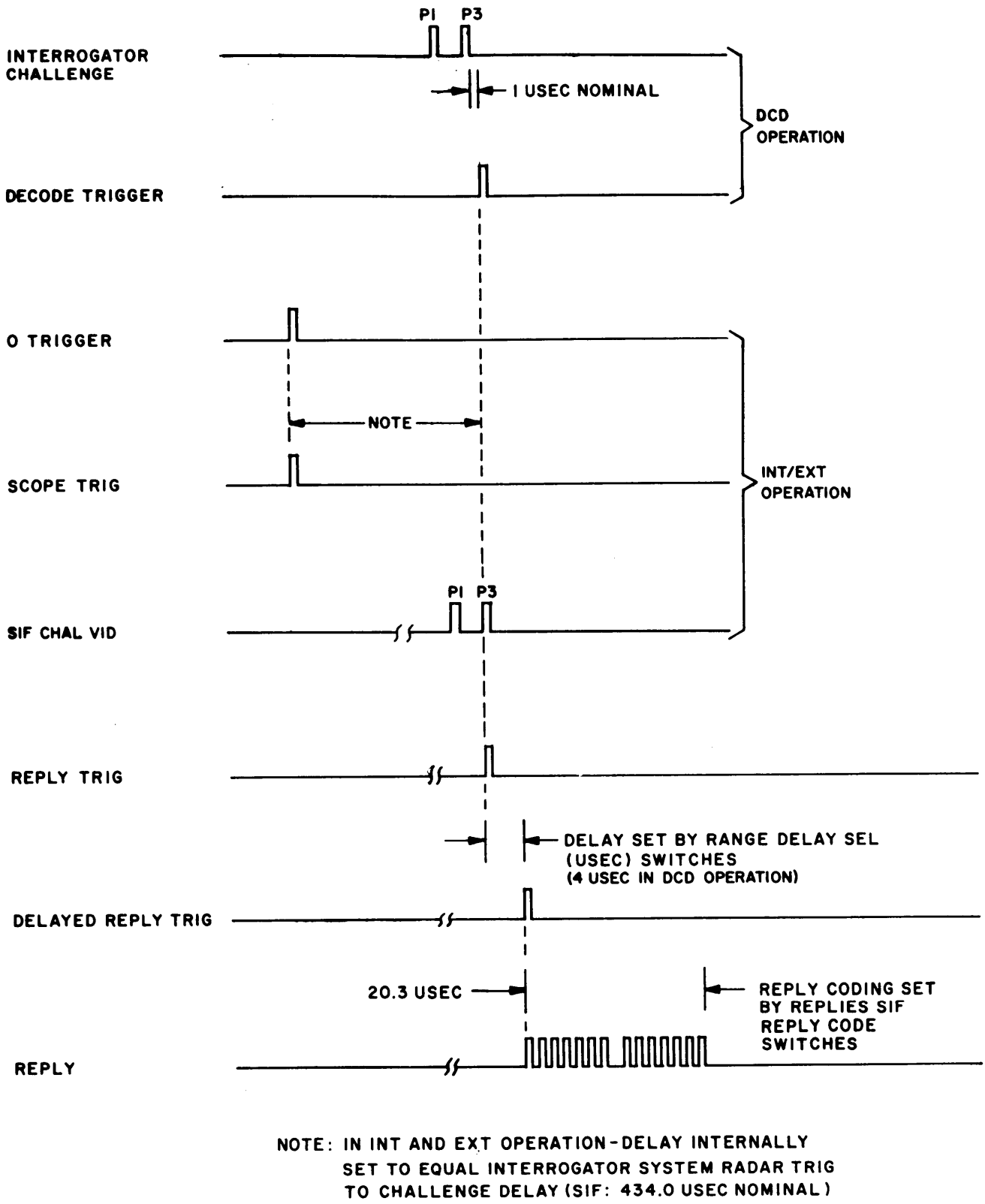

Figure 2-3 SIF fixed frequency trigger timing.

tion of the following SIF replies.

(a) SIF - normal SIF reply with framing pulses and selected information pulses.

(b) I/P Ml – identification of position in mode 1 with two sets of framing pulses and selected information pulses.

(c) I/P M 2/3 - identification of position in mode 2 with normal SIF reply plus an additional pulse in the SPI position.

(d) EMERG - emergency reply with normal SIF reply plus three additional sets of framing pulses.

(e) GARBLE - a simulated garble condition with a normal SIF reply plus one additional pulse spaced 20.3 µsec from a selected substituted information pulse. The position is selected by the REPLIES SUB PULSE SEL and varied by the REPLIES SUB PULSE POS. The Reply Video Generator Section generates sum and difference modulation video. Sum and difference modulation video signals modulate the fixed frequency rf (1090 MHz) within the dual modulator in the RF Generator Section to form the reply rf signals which appear at the SUM and DIFF RF IN/OUT jacks. The buffered sum modulation video from the Reply Video Generator Section is also applied to the REPLY VID OUT jack. Video at the REPLY VID OUT jack can be used to check the reply video processing circuits of the interrogator. When the SIG GEN switch is set to NORM, identical signals are applied to the SUM and DIFF RF IN/OUT jacks. Power level of the reply rf signals is controlled by the SUM and DIFF/INTERLEAVE ATTEN controls. (The reply rf signals are used to check the receiver and reply processing circuits of the interrogator.) When the SIG GEN switch is set to INTERLEAVE the difference modulation video is delayed 0.7 µsec from the sum modulation video. The rf outputs are combined and appear at the SUM RF IN/OUT jack. (In this manner the interleave capability of the interrogator can be tested). The DIF/INTERLEAVE ATTEN control varies the amplitude of the delayed interleaved reply rf signal (relative to the sum reply rf signal), The SUM ATTEN control adjusts the power level of both rf outputs. The challenge rf signal generated by the interrogator under test, initiated by the signal at the test set RDR TRIG OUT jack, is applied to the SUM and DIFF RF IN/OUT jacks. The challenge rf signals are applied to the receiver coupler, then detected and combined in the detector amplifier, The output of the detector amplifier is amplified and provided at the MEASUREMENT DEMOD VID OUT jack for display on the external oscilloscope. When the MEASUREMENT FUNCTION SEL switch is set to PRF EXT, the prf of the signal applied to the EXT VID IN jack is indicated by the MEASUREMENT meter. When the MEASUREMENT FUNCTION SEL switch is set to PRF REPLY TRIG, the MEASUREMENT meter indicates the prf of the reply trigger signal. With the switch in the PRF CHAL position the meter indicates the PRF of the interrogator challenges. When the MEASUREMENT FUNCTION SEL switch is set to PWR, the MEASUREMENT DEMOD VID LEVEL control is used to control the amplitude of the signal at the MEASUREMENT DEMOD VID OUT jack. The output of the control is also applied to the measurement section to cause an indication on the MEASUREMENT meter. When the DEMOD VID LEVEL control is adjusted so that the signal at the MEASUREMENT DEMOD VID OUT jack is 1.0 volts in amplitude, the MEASUREMENT meter indicates the input rf power level.

f. Mode 4 Fixed Frequency Operation. The simplified block diagram for mode **4** operation is shown in figure 2–4. Mode 4 timing is described in figures 2–5 and 2–6.

(1) *Mode 4 challenge pulse generation* (fig. *2-5).* In the same manner as described for SIF operation the PRT Generator and Output Trigger Generator Sections develop a radar trigger (RDR TRIG) and oscilloscope trigger (SCOPE TRIG). In the Output Trigger Generator Section, the mode *4* challenge video generator gates the 500 KHz stop signals. The M4 start signal which occurs 168 µsec after the M4 int ref signal, generates the video at the MODE 4 CHAL VID OUT jack. The pulses at the MODE 4 CHAL VID OUT jack are 0.5 psec in duration into a 90 ohm load. Upon receipt of the M4 start signal, the mode 4 challenge video generator begins gating 500 KHz clock pulses which appear at the MODE 4 CHAL VID OUT jack. The first four pulses are gated out as mode 4 sync pulses. The fifth pulse is inhibited by the M4 ISLS gate which occurs 176 µsec after the M4 int ref signal. The mode 4 challenge video generator then gates out 32 pulses which simulate mode **4** challenge video. Generation of the challenge video is stopped upon receipt of the M4 stop signal which occurs at 242 µsec after the M4 int ref signal. At 372 µsec after the M4 int ref signal, the M4 GTC signal is applied to the M4 GTC shaper (fig 2–4, sh 2) to develop the signal at the MODE 4 GTC TRIG OUT jack. This signal triggers the GTC function of the interrogator.

(2) *Mode 4 reply generation.* After a delay the reply trigger is generated by the PRT Generator Section. The delay between the 0 trigger and the reply trigger (normally 449.0 µsec) is internally set to equal the radar trigger to challenge delay of the type interrogator under test. The reply trigger is applied to the Delay Generator Section. It delays the reply trigger by the interval set into the RANGE DELAY SEL (µSEC) switches. Reply gating is accomplished in the Replies Gating Pass Inhibit operation as in SIF operation, as previously described. The delayed reply trigger from the Delay Generator Section is applied to the Reply Video Generator Section to trigger a re-

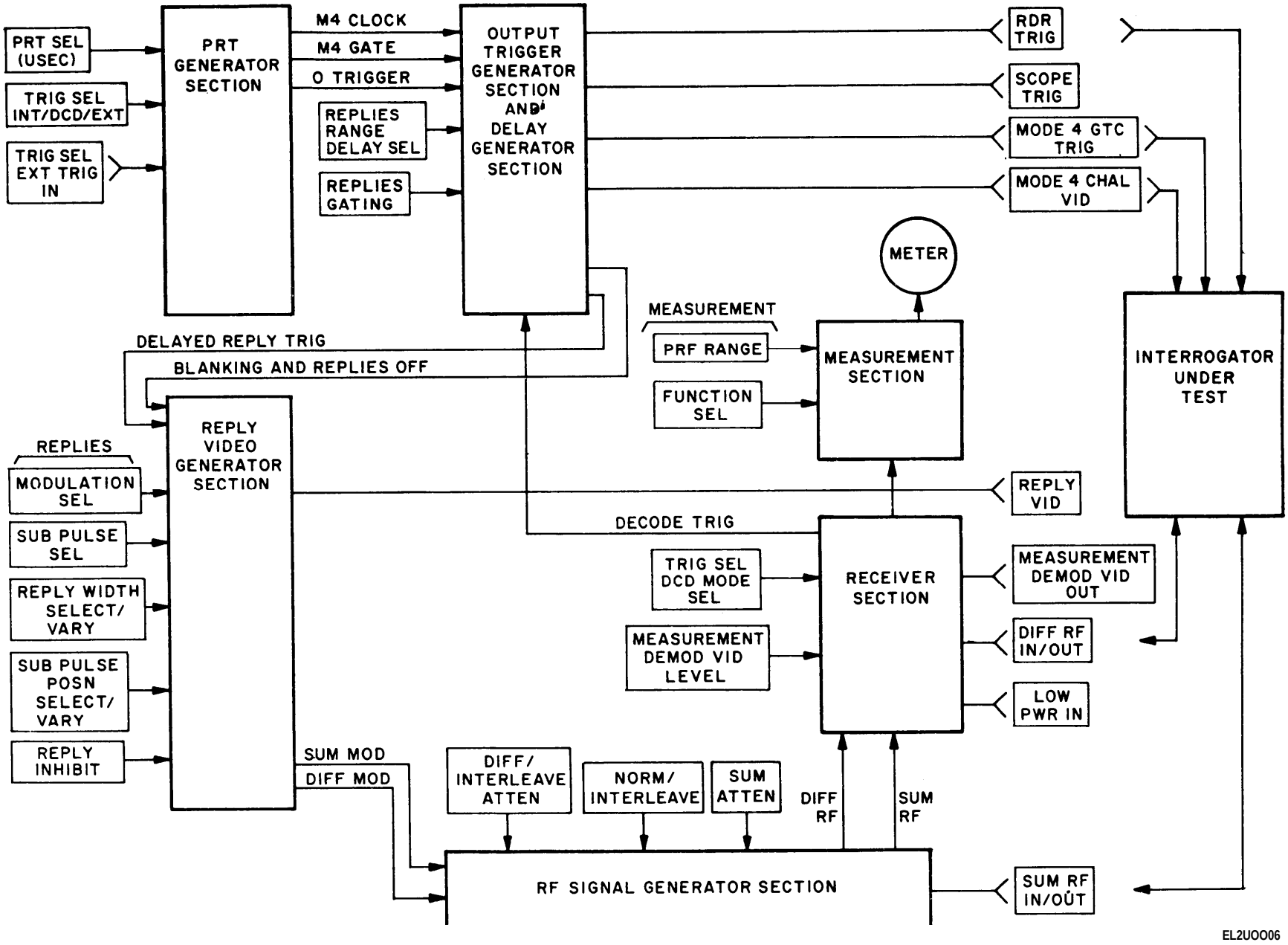

Figure 2-4. Mode 4 fixed frequency, simplified block diagram (sheet l of 2).

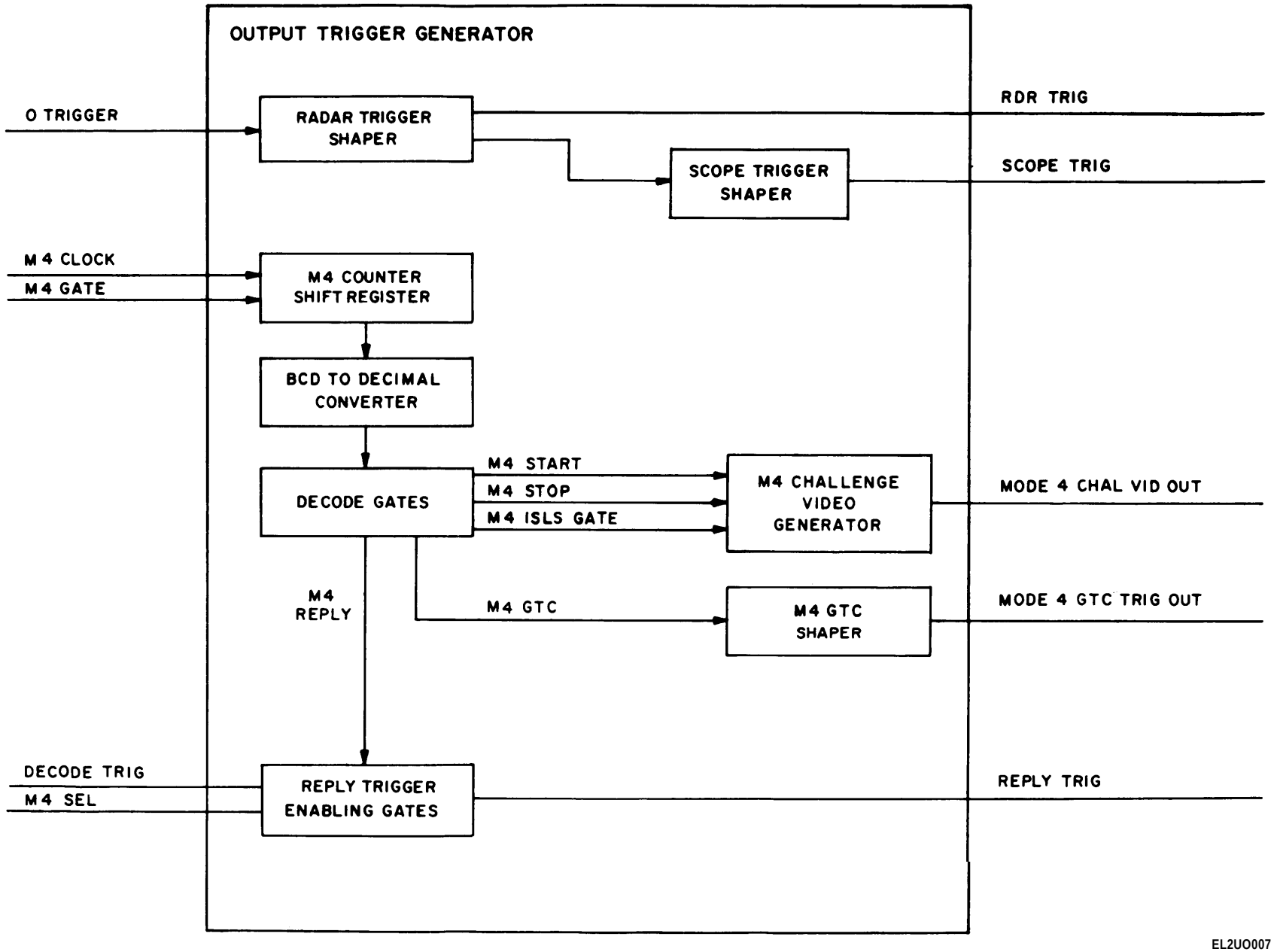

Figure 2-4. Mode 4 fixed frequency, simplified block diagram (sheet 2 of 2).

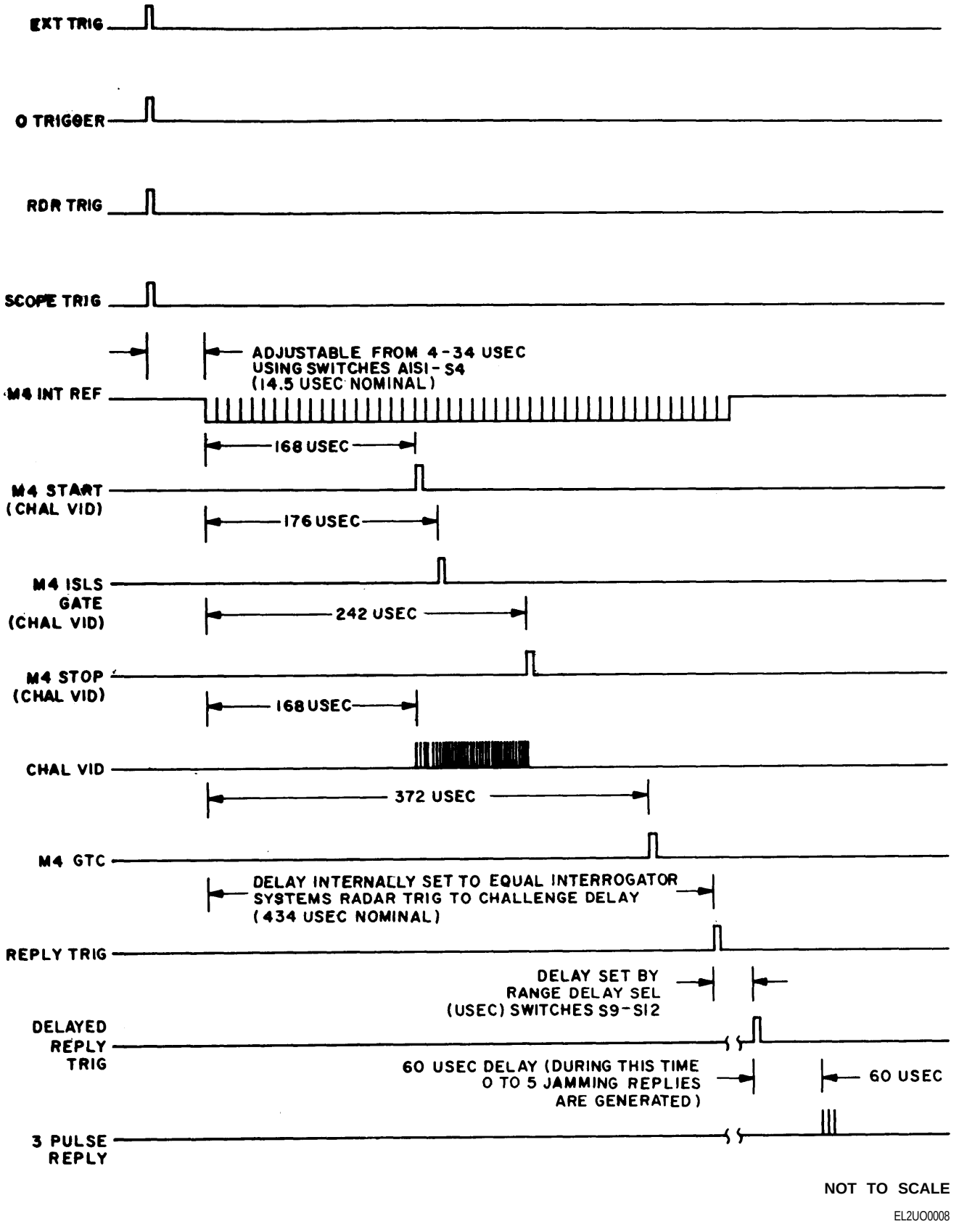

Figure 2–5. Mode 4 fixed frequency trigger timing.

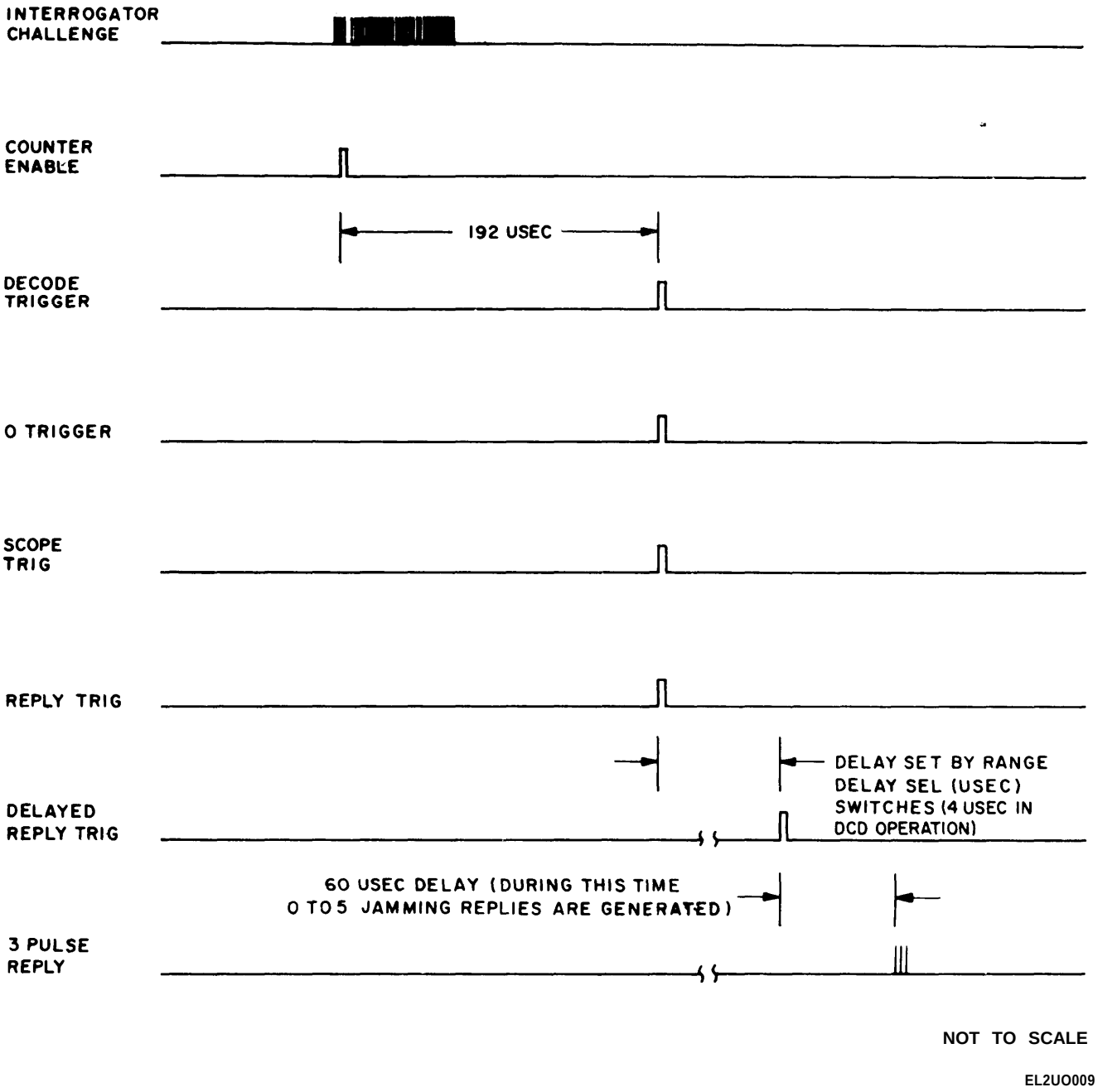

Figure 2–6. ***Mode*** *4* ***fixed*** *frequency trigger tinting* ***(DCD).***

ply. The type of reply is determined by the REPLIES MODULATION SEL switch which selects either a 3-pulse reply or a l-pulse reply. Positioning of P2 or P3 pulses within the 3-pulse reply can be varied using the REPLIES SUB PULSE controls. The Reply Video Generator Section generates sum and difference modulation video, Sum and difference modulation video signals modulate the **1090** MHz fixed frequency rf within the dual modulator of the RF Signal Generator Section signals which appear at the SUM and DIFF RF IN/OUT jacks. The Reply Video Generator Section generates a reply video approximately 60 µsec after the receipt of a delayed reply trigger. During the 60 µsec period, the reply video generator and consequently the rf output from the test set can generate from O to 5 jamming replies. (The sum modulation video at the REPLY VID OUT jack can be used as the time decoded video input to the interrogator as well as for checking the reply video circuits of the interrogator). The rest of the test set operates as described previously. In DCD operation the receiver functions as previously described for

SIF operation, except for the criteria to generate the decode trigger. Refer to figure 2–6 for DCD timing. A trigger is generated upon receipt of the four mode 4 challenge sync pulses. The decode trigger is delayed 192 µsec by the challenge decoder. This delay, combined with approximately 6 µsec to decode the sync pulses and 60 µsec delay between the delayed reply trigger and the reply itself provides approximately 259 µsec total delay. The 259 µsec delay is provided to simulate the challenge to the reply delay of the mode 4 KIT and KIR computers and transponder turnaround time.

2-4. Swept RF Operation

(fig. 2-7)

The swept rf operation mode is used to check interrogator receiver bandwidth and transmitter frequency characteristics. The test set varies the rf frequency of the replies generated to check interrogator receiver bandwidth, To measure interrogator transmitter frequency the test set compares the interrogator challenge rf with a sweeping calibrated local oscillator. When the SIG GEN FUNCTION switch is set to SWP ± 5 MHZ (to check interrogator challenge rf frequency), the RF Signal Generator Section develops a swept rf. The rf sweeps from 1085 to 1095 MHz, The rf generator section then provides markers corresponding to 1085, 1089, 1090, 1091 and 1095 MHz. When the SIG GEN FUNCTION switch is set to SWP +15 MHZ (to check interrogator receiver bandwidth) the rf sweeps from 1075,1080,1085, 1089, 1090,1091,1095, 1100, and 1105 MHz. Each marker is generated at the time the rf sweep is at the corresponding frequency. The swept rf is divided within the dual modulator to provide two separate rf outputs which are modulated by the sum and difference modulation video signals from the reply video generator. The modulated rf outputs are applied to the SUM AND DIFF RF IN/OUT jacks through the SUM and DIFF/INTERLEAVE ATTEN controls. When the test set is set to swept mode the 0 trigger signal is delayed and generates a scope trigger signal at the SCOPE TRIG jack. The amount of delay is controlled by the MEASUREMENT FREQ MEAS control. At the same time a scope trig output occurs, a sweep start signal is sent to the ramp generator circuits in the RF Signal Generator Section. A ramp signal is generated which causes the test set rf output signal to be swept from 1075 to 1105 MHz (SWP ±15 MHZ) or from 1085 to 1095 MHz (SWP ± 5 MHZ). At the conclusion of the sweep signal an additional 400 µsec delay is set, after which the sweep can be retriggered by another delayed 0 trigger signal. Retriggering of the ramp generator is inhibited during the period of the sweep by the absence of a SWEEP CLOCK SYNC output from the ramp generator in the RF Signal Generator Section. The source of the PRF of the 0 trigger can be either the internally selected PRF from the PRT SEC (µSEC) switches, the external trigger from the TRIG SEL EXT TRIG IN jack or a decoded challenge from the interrogator under test. This is explained previously in paragraph 2–3a, b, and *c*. Coincident with the 0 trigger a reply trigger is generated. This trigger is delayed by the Delay Section and causes generation of the reply video as previously described for fixed frequency operation. The delay between the triggered reply video and the start of the swept rf output is controlled by adjusting the MEASUREMENT FREQ MEAS control. In this manner the time at which the reply is generated is selected and the frequency of the reply is also determined. The longer the delay of the sweep start signal, the lower the rf frequency of the reply, since the reply video modulates the rf earlier in the sweep. By adjusting the MEASUREMENT FREQ MEAS control replies can be made at different frequencies and the interrogator receiver bandwidth determined. The nominal frequency of the interrogator transmitter is 60 MHz below the nominal test set rf generator output. The incoming challenge rf signal from the interrogator (always synchronized with the test set radar trigger output as described for fixed frequency operation) is attenuated and mixed with the swept cw test set rf generator output. The mixer output is jittered and amplified at 60 MHz (1090 MHz nominal – 1030 MHz nominal). This signal is detected and provided as a test set output at the MEASUREMENT DEMOD VID OUT when the MEASUREMENT FREQ MEAS control causes triggering of the swept rf ramp at selected delays with respect to the interrogator challenge. In this manner the challenge position is adjusted until a peaked signal output is observed at the MEASUREMENT DEMOD VID OUT jack, The position with respect to the swept rf of the challenge is accurately 60 MHz; hence a 1032 MHz challenge corresponds to a 1092 MHz position on the test set rf sweep. By observing the test set markers position and MEASUREMENT DEMOD VID OUT signal the corresponding interrogator transmitter frequency is determined.

a. Transmitter Frequency Testing (fig. 2–8). When measuring interrogator transmitter rf frequency, the challenge from the interrogator is applied to the input of the test set receiver through the SUM and DIFF RF IN/OUT jacks. The delay of start of the sweep with respect to the radar trigger and corresponding interrogator challenge is adjusted using the MEASUREMENT FREQ MEAS control until the challenge signal is 60 MHz from the instantaneous value of the swept rf. This is accomplished by adjusting the MEASUREMENT FREQ MEAS control until the detected challenge video peaks, as observed at the MEASUREMENT DEMOD VID OUT jack. The position of the challenge is then compared with the

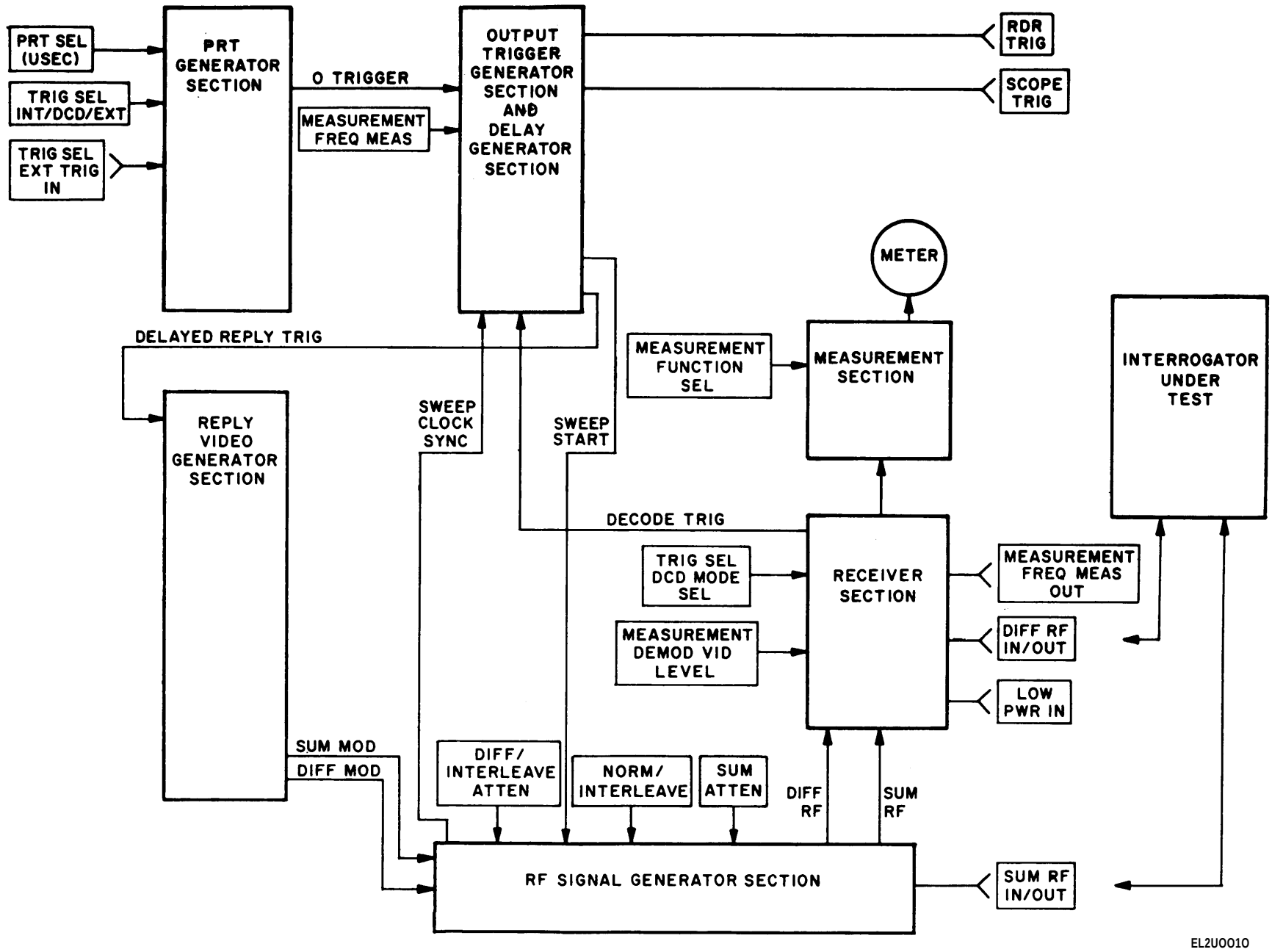

Figure 2-7. Swept frequency, simplified block diagram

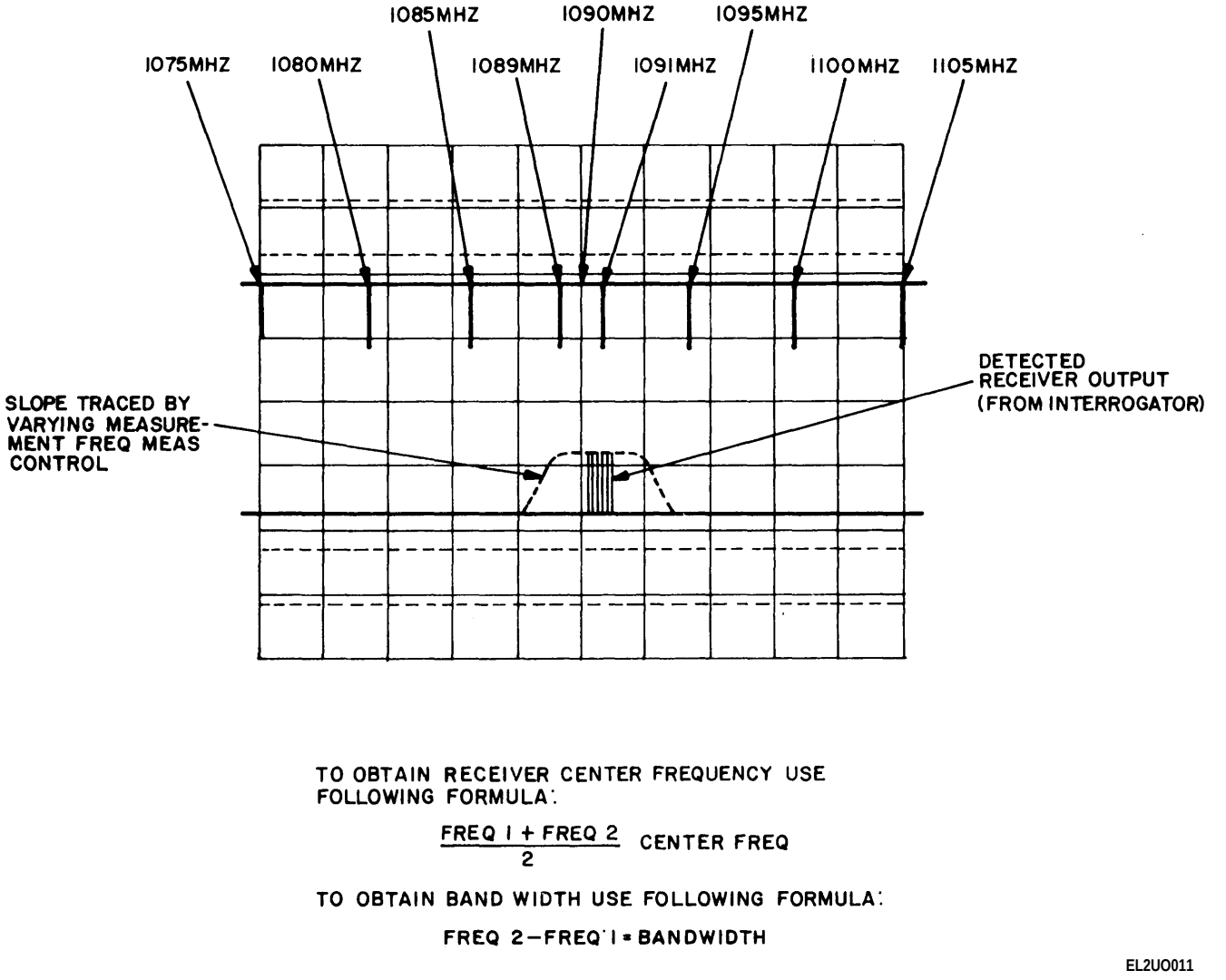

Figure 2-8. Transmitter frequency meaurement oscilloscope display

frequency marker video as shown in figure 2–8 to determine the challenge rf frequency. Because the challenge rf is displaced 60 MHz from the swept rf, the markers correspond to 1025,1029,1030, 1031, and 1035 MHz for transmitter frequency measurement.

b. Receiver Bandwidth and Center Frequency Testing (fig. *2–9).* When measuring interrogator receiver bandwidth and center frequency, the MEASUREMENT FUNCTION SEL switch is set to PRF CHAL. The interrogator detected receiver video is observed directly. The start of sweep is adjusted, using the MEASUREMENT FREQ MEAS control until the detected reply signal is displayed. The replies are varied in frequency and attenuated until the frequency of maximum interrogator receiver sensitivity is determined. The SUM AT TEN (or DIFF/INTERLEAVE ATTEN for interrogator difference channel bandwidth measurement) is adjusted until MTL (minimum triggering level) is achieved by observing a reply rate of 90% of the challenge prf when the MEASUREMENT FUNCTION SEL switch is set to PRF REPLY TRIG as observed on the MEASUREMENT meter. At this time the SUM ATTEN (DIFF INTERLEAVE ATTEN) is decreased in attenuation by 6 dB. The MEASUREMENT FREQ MEAS control is adjusted to each of two points at which MTL is again obtained. At these points the oscilloscope is used to measure the frequencies. The formula shown is then used to locate the receiver center frequency. The REPLIES MODULATION SEL switch can also be set to CW or 30 KHZ which provides continuous sweeping rf from the dual modulator, the display then provides a full pattern of the receiver response.

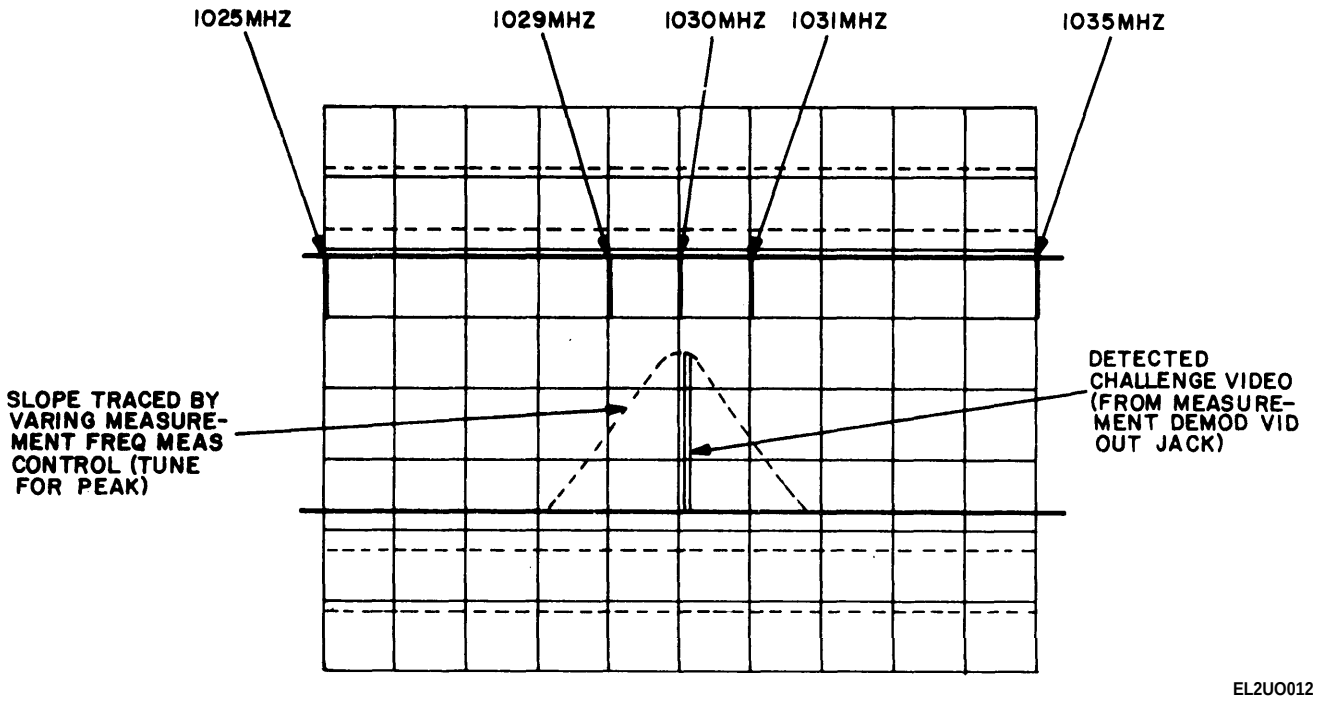

Figure 2-9. Receiver bandwidth measurement oscilloscope display.

c. *Self Test.* By jumping from the SUM or DIFF RF IN/OUT jacks to the LOW PWR IN jack the test set will receive its own signals for display on the oscilloscope at the MEASUREMENT DEMOD VID OUT jack. This permits testing of all circuitry within the test set except for the frequency measurement circuitry (i.e. mixer, 60 MHz if amplifier/filter and SIF decoder), The self test circuit is activated by pressing the BIT (MOM) switch, The test set rf generator output frequency is checked by checking the reference 1030 MHz signal frequency that is enabled during self test. The procedure is similar to the testing of the interrogator's transmitter frequency. To perform self test of the SIF Decoder in the Receiver Section the BIT (MOM) is pressed and the SIF CHAL VID SIF MODE SEL switch is stepped through the SIF modes while the TRIG SEL DCD MODE SEL is set to the corresponding mode positions. When both switches are selected in the same mode an SIF reply signal appears at the MEASUREMENT DEMOD VID OUT jack, Test set power output can be self-tested by setting the selected test set attenuator level (SUM or DIFF/INTERLEAVE) to a given level and performing a procedure similar to that used to make interrogator transmitter power measurements. A complete self test procedure is contained in TM 11–6625–2610–12.

Section III. BLOCK DIAGRAM DISCUSSION

2 – 5. General

fig. (FO-2)

The test set is composed of seven basic sections: the prt generator, the reply video generator, the output trigger generator and delay generator, the receiver, the rf signal generator, the measurement section, and the power supply.

2-6. PRT Generator

(fig. FO-2)

The prt generator develops clock and trigger signals for use in the reply video generator and provides a time base for the output signals of the output trigger generator. Zero (0) triggers are generated in response to trigger pulses from the TRIG SEL EXT TRIG IN jack, decode trigger signals from the receiver, or from timing signals generated within the prt generator itself. At the beginning of each cycle, the prt generator generates the various timing triggers for the output trigger generator. The PRT SEL (µSEC) switches select the time interval between O triggers. A chart is supplied with the test set which has a graph for conversion of PRT to PRF.

2-7. Output Trigger Generator (fig. FO-2)

a. The output trigger generator provides various outputs to the front panel jacks in response to the timing triggers from the PRT Generator Section. The radar trigger occurs at 0 trigger time each time the prt generator is triggered. Infixed frequency operation the scope trigger also occurs at 0 trigger time. Upon receipt of a 0 trigger and a 10 MHz clock signal (clock (10)) the output trigger generates an SIF pretrigger from the SIF CHAL VID SIF PRE TRIG OUT jack. The delay between the 0 trigger and SIF pre trig signal is nominally 386 µsec and is adjustable on the Al card. An SIF gate signal is similarly delayed (adjustable on the Al card) and with an SIF clock signal generates the SIF chal trig signal (Pl and P3 triggers). The spacing of the SIF chal trig pulses is determined by the position of the SIF CHAL VID SIF MODE SEL switch. The sif chal trig signal is then buffered and provided as an output signal at the SIF CHAL VID CHAL VID OUT jack. The signal at the SIF CHAL VID CHAL VID OUT jack is selected as a 5 volt amplitude signal by the SIF CHAL VID 20V/5V switch, The PRT generator also provides the timing marker output signals. The 10 MHz (100ns) signal along with 1 MHz (1µs), 100 Khz (10µs), and 10 KHz (100µs) signals are added together to provide a composite timing markers output signal from the MEASUREMENT TIMING MKRS OUT jack. The 10 KHz markers are of the greatest amplitude and the other markers decrease in amplitude as the frequency increases.

b. In swept frequency operation, the 0 trigger is delayed to start the rf sweep. The delay between 0 trigger and the delayed scope trigger (sweep start) is set by the MEASUREMENT FREQ MEAS control. If the time between successive 0 triggers is less than the time required to complete the sweep of the rf generator, the clock sync signal inhibits generation of a sweep start trigger until the sweep is complete.

c. A reply trigger is generated as follows:

(1) Upon receipt of an M4 reply trigger with an M4 sel signal in mode 4 operation.

(2) Upon receipt of a decode trigger with a decode enable trigger in DCD operation.

(3) With an sif sel signal, 3 µsec after the sif chal trig signal is completed (P3 has been triggered) and is selected for SIF operation without challenge decoding (DCD) enabled.

d. Upon receipt of a reply trig signal, the Delay Generator Section generates a delayed reply trig signal. The delay between the reply trig and delayed reply trig signals is selected by the REPLIES RANGE DELAY SEL switches. The total delay in SIF operation between the 0 trigger and the delayed reply trig signals is the sum of the preset SIF delay (434 µsec nominal) and the delay selected by the REPLIES RANGE DELAY SEL switches, except in DCD operation where the preset SIF delay is decreased to 4 µsec.

e. The Delay Generator Section also contains logic which alternately enables and then inhibits reply generation as determined by the REPLIES GATING PASS and INHIB switch settings. The REPLIES GATING PASS and INHIB switches can be set to any combination from 01 to 99. The delay generator then consecutively enables the number of replies set into the REPLIES GATING PASS switches. Once the number of replies on the REPLIES GATING PASS switches has been reached, the number of replies set into the REPLIES GATING INHIB switches is inhibited. If the REPLIES GATING INHIB switches are set to 00, reply video and reply rf outputs are enabled all the time, regardless of the setting of the REPLIES GATING PASS switches.

f. The timing of the mode 4 out signal is referenced to the mode 4 internal timing reference (M4 int ref) (fig. 2–5). The M4 int ref signal is adjustable with respect to 0 trigger, between 4 and 34 µsec, and is nominally set to 14.5 µsec. The mode 4 out challenge video pulse train occurs 168 µsec after the M4 int ref signal and consists of 37 pulses spaced 2.0 µsec apart, with the exception that the pulse normally spaced 8.0 µsec from the first, is inhibited. The mode 4 GTC trigger occurs 372 µsec after the M4 int ref signal.

2-8. Reply Generator Section

a. Upon receipt of the delayed reply trigger, the reply generator develops a reply video signal. The reply video signal is available at the REPLY VID OUT jack for display on the oscilloscope. The reply video signal also develops the sum and difference modulation drive applied to the rf signal generator. The REPLIES MODULATION SEL switch selects the type of reply video generated, with the REPLIES MODULATION SEL switch set to SIG, the 20-MHz clock is divided by 29 to obtain a 1.45 µsec clock pulse. For each delayed reply trigger received, a reply train of up to 14 pulses is generated. The REPLIES SIF REPLY CODE switches determine the reply code. Setting the REPLIES MODULATION SEL switch to I/PMl causes the Reply Generator Section to generate two complete reply pulse trains for each delayed reply trigger signal received, spaced 4.35 µsec apart. In the I/P M2/3 position, the normal reply pulse train is followed by an identification pulse. In the EMERG mode, the reply pulse train is followed by three sets of bracket pulses. In the GARBLE mode, the reply pulse train contains an extra pulse spaced 20.3 µsec from the substitute pulse selected with the REPLIES SUB PULSE SEL switch. With the REPLIES MODULATION SEL switch set to M4–1P or M4–3P, the 20-MHz clock is divided by 80

to provide a 4.0 µsec clock pulse. In mode 4 operation, a 1- or 3-pulse reply is selected with the REPLIES MODULATION SEL switch and generated by the Reply Generator Section. The REPLIES M4 JAMMING switch selects up to five sets of synchronous jamming replies to be generated and added to the selected mode 4 reply.

b. The sum and difference modulation video signals are generated separately and with the SIG GEN NORM/INTERLEAVE switch set to NORM, the modulated sum and difference reply rf signals are applied simultaneously to their respective RF IN/OUT jacks. When the SIG GEN NORM/INTERLEAVE switch is set to INTERLEAVE, the modulated signals occur 0.7 µsec apart and both are applied to the SUM RF IN/OUT jack.

c. When the REPLIES MODULATION SEL switch is set to 30 KHz, reply pulses are generated continuously at a 30-KHz rate. When the REPLIES MODULATION SEL switch is set to CW, modulation is inhibited and the RF Signal Generator Section provides unmodulated cw rf outputs. The reply video pulse width is controlled by the REPLIES REPLY WIDTH SELECT or VARY controls. A variable position substitute pulse, selected by the REPLIES SUB PULSE SEL switch, can be substituted for the pulses in the reply video. The position of the pulse, in respect to normal pulse position, is varied by the REPLIES SUB PULSE POS SELECT and VARY controls.

2 – 9. RF Signal Generator Section

a. The RF Signal Generator Section generates fixed frequency rf at 1090 MHz, or swept frequency rf varying from 1085 to 1095 MHz or 1075 to 1105 MHz, modulated by the sum and difference modulation video signals from the reply generator section. It also provides the local oscillator rf signal to the receiver which is mixed with the incoming rf from the interrogator under test to measure the interrogator transmitter frequency. In swept frequency operation, the RF Signal Generator Section generates sweep frequency markers which correspond to 1025, 1029, 1030, 1031, and 1035 MHz for ±5 MHz sweep and 1075, 1080, 1085, 1089, 1090, 1091, 1095, 1100 and 1105 MHz for ±15 MHz sweep.

b. In either swept or fixed frequency operation, the reply video generator sum and difference modulation video signals modulate their respective reply rf outputs. With the SIG GEN NORM/INTERLEAVE switch set to NORM, the sum rf is applied to the SUM RF IN/OUT jack, and the difference rf to the DIFF RF IN/OUT jack. If the SIG GEN NORM/INTERLEAVE switch is set to INTERLEAVE, the difference and sum rf signals are combined and applied to the SUM RF IN/OUT jack. The DIFF/INTERLEAVE ATTEN control adjusts the amplitude of the difference rf with respect to the sum rf level and the SUM ATTEN control determines the overall level of the rf at the SUM RF IN/OUT jack.

c. Pressing the BIT (MOM) switch in swept frequency operation, activates an internal self-test rf generator operating at 1030 MHz whose output is mixed with the rf generator local oscillator signal. The resultant signal provides a self-test of portions of the RF Signal Generator, Receiver, and Measurement sections. Pressing the BIT (MOM) switch also provides capability to test the interrogator challenge decoder in the receiver section.

2-10. Receiver Section

The Receiver Section accepts signals from the interrogator under test through the SUM and DIFF RF IN/OUT jacks. Signals less than +10 dBm (such as test equipment outputs) are applied to the LOW PWR IN jack. The LOW PWR IN jack is also used to check the output of the test set itself during self-test. The rf applied to either of the RF IN/OUT jacks is coupled to both of the receiver demodulators. One demodulator is the detector amplifier which preserves video pulse fidelity, and during power measurements the output video observed at the MEASUREMENT DEMOD VID OUT jack is adjusted for a standard 1 volt amplitude using the MEASUREMENT DEMOD VID LEVEL control. A signal from the MEASUREMENT DEMOD VID LEVEL control is also applied to the measurement section and the input peak power level is indicated on the meter. The other demodulator mixes the rf output from the rf generator with the incoming rf and the resultant signal is applied to a 60 MHz if amplifier. During swept frequency operation, any rf signal 60 MHz away from the rf generator frequency is amplified and detected and appears at the MEASUREMENT DEMOD VID OUT jack. The MEASUREMENT FUNCTION SEL switch determines which demodulator output is selected and which function is displayed on the meter or oscilloscope. In decode enabled operation (DCD), the received interrogator challenge signal triggers the test set reply. If the pulse spacing of the mode selected by the DECODE SELECTION switches corresponds to the challenge pulse spacing, the receiver applies a decode trigger to the Output Trigger Generator Section which then triggers a reply. During self-test, for pulse fidelity or power checks the SUM or DIFF RF IN/OUT jack is connected to the LOW PWR IN jack. The resultant signal is then available at the MEASUREMENT DEMOD VID OUT jack for display on the oscilloscope.

2-11. Measurement Section

The Measurement Section accepts reply prf from the PRT Generator Section, signals from the Receiver Section, and pulses from the MEASUREMENT EXT

VID IN jack. The input to be measured is selected with the MEASUREMENT FUNCTION SEL switch. The output of the measurement section is applied to the MEASUREMENT meter for display, and the meter scale factor is set by the MEASUREMENT PRF RANGE switch.

2-12. Power Supply

The power supply receives primary power (115 v, 60 or 400 Hz) through the POWER IN connector and develops the dc voltages necessary to operate the test set. Power is applied through the POWER ON/OFF switch. The power supply input is fused to provide overload protection and a neon lamp on the fuseholder lights if the fuse opens. Should any of the power supply outputs malfunction, the POWER DC FAULT indicator lights to indicate a malfunction. Each power supply output is current limited to provide for circuit overload protection. The POWER DC FAULT indicator has a PRESS TO TEST action which provides a self-test of the indicator.

Section IV. DETAILED DESCRIPTION

2-13. PRT Generator Section
(fig, FO-3)

The PRT Generator Section develops the following trigger and clock signals to synchronize the time the test set operations and outputs: the 0 trigger which establishes the basic prt of the test set; the reply trigger which is delayed and used to trigger the SIF and mode 4 replies in the Reply Generator Section; 10 and 20 MHz clock signals used throughout the test set to synchronize and time test set outputs; mode 4 triggers used to generate simulated mode 4 computer outputs in the Trigger Generator Section; and SIF pretriggers and challenge pulse pairs. The 0 trigger is generated by one shot A1U11. This one shot can be triggered internally, externally or by a decoded interrogation.

a. Internal Trigger Operation. Internal trigger operation is initiated by setting the TRIG SEL switch to INT. For this operation, the repetition rate of the 0 trigger, which determines the test set prf, is established internally. Generation of the delayed reply trigger, which establishes the timing and delay of the SIF or mode *4* replies, depends on the position of the TRIG SEL DCD MODE SEL switch. If the test set is operated with this switch OFF (internal trigger without decode enabled operation), the delayed reply trigger is generated in response to the 0 trigger. With this switch in any of the modes, (internal trigger with decode enabled operation), the delayed reply trigger is generated in response to a decode trigger obtained by decoding the challenge from the interrogator under test. Generation of the 0 trigger is described in (1) through (3) below. Paragraphs (1) and *(2)* below provide a functional description of the internal trigger without decode enabled operation for SIF and mode 4 respectively. Paragraph *(3)* below provides a functional description of internal trigger with decode enabled operation (SIF and mode 4). The 0 trigger is generated by a closed loop consisting of prt counter A1U4–U8, prt select comparator AlU13/U15/U17/U19, internal trigger gate A1U10A, start trigger gate A1U9A, and 0 trigger generator one-shot A1U11. When TRIG SEL switch S24 is set to INT, gate A1U10A is enabled through inverter A1U1B. Prt counter A1U4–U8 is continually advanced by the 10 MHz clock signals generated by crystal-controlled system clock A2Y1/Q1/Q2/U2C. BCD outputs representing the instantaneous count of the prt counter are applied to prt select comparator A1U13/U15/U17/U19. BCD inputs from the PRT SEL (µSEC) switches S5-S8 are compared to the BCD outputs of the prt counter with the comparator A1U13/U15/U17/U19 to determine the pulse repetition time (prt) of the test set. The PRT SEL (µSEC) switches can be set for 500 to 9999 µsec. When the prt counter reaches the selected prt, that is, when the prt counter BCD signals equal the prt select BCD, the prt select comparator outputs go high, and are applied to A1U10A through A1U10/U9B. The output of internal trigger gate A1U10A goes low, triggering 0 trigger generator one-shot A1U11 through A1U9A. The 0 trigger resets all but the first stage of the prt counter and the loop operation is repeated. The 0 trigger is supplied to the output trigger generator to generate the radar trigger output at the test set RDR TRIG OUT jack, and in fixed frequency mode of operation, the scope trigger at the MEASUREMENT SCOPE TRIG OUT jack. In addition, the 0 trigger is applied to the Reply Generator Section and the Measurement Section. The trailing edge of the 0 trigger sets flip-flop U20C/D. It is reset by the reply trig (either SIF or M4) to form the max prf gate. The max prf gate is used to prevent PRT/range overlay.

(1) *Internal trigger without decode enabled.* The 0 trigger is internally established as described above. With the REPLIES RANGE DELAY SEL switches set for 0001, the SIF reply (REPLY VID OUT or reply at SUM or DIFF RF IN/OUT) can be adjusted to occur from 360 to 438 µsec after the 0 trigger by A1S4, S5 and S6. The mode 4 reply (at DIFF or SUM RF IN/OUT) can be adjusted to occur *430* to *464 µsec* after the 0 trigger. In practice these delays are set to match the system delays under test. The prt counter

BCD output pulses are developed from 5 decade counters, representing tenths, units, tens, hundreds, and thousands of microseconds. The 10 MHz clock signal and the output of each of the first three decades are summed from A1U3A, B, C, and D to provide timing markers at MEASUREMENT TIMING MKRS OUT jack J17. For easy identification, the amplitude of each decade output increases with the significance of the decade (0.1 µsec is the smallest and 100 µsec the largest). Timing markers are provided whenever the test set is turned on. As the prt counter advances, the BCD output pulses are applied to BCD-to-decimal converters AlU12/U14/U16/U18 to generate decimal coded timing outputs. There are three types provided; mode 4 timing, SIF timing, and SIF pretrigger timing. The BCD-to-decimal converter output is the decimal equivalent of the instantaneous BCD input. The decimal coded timing signals are applied through SIF reply minimum delay adjust switches A1S4, S5, and S6 to SIF gate and clock decode gates A1U21A and A1U20B. These signals are also applied through mode 4 reply minimum delay adjust switches A1S1, S2, and S3 to M4 gate and clock decode gate A1U20A and A1U22A. These signals also are applied through SIF PRE TRIG delay adjust switches A1S7, S8, and S9 to SIF PRE TRIG decode gate A1U21B. The sif pre trig is adjustable with respect to the 0 trigger signal over a range of from 301 to 398 µsec. Each of the switches is preset to p pass one of the inputs applied. For example, switch A1S4 can be set to pass one of the tenths digits, A1S5 one of the units digits, and so on (fig. FO–3, sh 3). Counters A1U14 and U15, and BCD-to-decimal converters A1U17 and U18, are also decoded by output trigger generator gates A1U20A, B, and C, and A1U21A, B, and C to provide SIF challenge triggers (sif chal trig signal). Upon receipt of an sif clock signal and an sif gate signal (if the SIF CHAL VID SIF MODE SEL switch is set to either modes 1, 2, 3, or C), triggers corresponding to pulse positions for P1 and P3 are generated as an sif chal trig signal (fig. FO–4). The sif chal trig signal is then shaped by A3U8B and provided through A3Q18, Q19, Q20, Q21, and Q22 as an SIF CHAL VID 5V or 20V output. In SIF operation, 48 µsec after sif gate and sif clock signals are generated, a reply trig signal is gated through A2U20B, U23D, and U18C. Delay counter latch A4U15A/U15B is set by the reply trig signal, enabling delay counter A4U16/U20. The range delay counter (fig. FO–3, sh 4), consists of five decades and is clocked at 10 MHz, The 1, 10, 100 and 1000 µsec counts and the end of the delay signal appear in the range counter composite signal at test point TPB8. The amplitude of each decade output increases with the significance of the decade (1 µsec is the smallest and 1000 µsec largest). The range delay counter BCD delay timing outputs are applied to range delay comparator A4U22/U25, and compared with the range delay time selected by the REPLIES RANGE DELAY SEL (µSEC) switches S9 through S12. The time selected, simulates the slant range of a transponder. When the range delay counter output reaches the selected range delay time, the delay comparator generates an end of delay count signal. The one-shot output from A4U4A is used to reset delay counter latch A4U15A and B terminating the range count and as a delayed reply trigger to drive the reply video generator.

Table 2–1. Decimal Coded Reply Timing Outputs

Tenths	*Units*	*Tens*	*Hundreds*
.0 µsec	0 µsec	00 µsec	000 µsec
.1	1	10	300 µsec
.2	2	20	500 µsec
.3	3	30	
.4	4	40	
.5	5	50	
.6	6	60	
.7	7	70	
.8	8	80	
.9	9	90	

(a) Prt/delay overlap error detection (fig. FO–3, sh 4). Prt/delay overlap sensor flip-flop A4U3B and error signal generator one-shot A4U4B are initially cleared through gates A4U6D and A4U6C respectively. When the 0 trigger is generated, the prt/delay overlap sensor flip-flop is clocked and set. Gate A4U6D is enabled when the max prf gate flip-flop is cleared by the reply trigger. During normal operation, the blanking reset signal clears the prt/delay overlap sensor flip-flop for the next reply cycle. If the range delay time plus the reply signal delay time is greater than the test set prt, a second 0 trigger is generated before the end of the reply cycle. The second 0 trigger triggers the error signal generator one-shot. The Q output of A4U4B goes low, enabling gate A4U5B and the generation of the blanking and replies off output. The error output drives lamp driver A4U5B and REPLIES REPLY INHIB indicator DSI lights. Error signal generator one-shot A4U4B inhibits normal operation for 2 seconds. If

before the end of that time, the error conditions are not corrected, the prt/delay overlap sensor flip-flop cannot be cleared and the error signal generator one-shot is again triggered by the next 0 trigger. The reply inhibit condition remains until the test set prt is increased, or the range delay decreased, establishing the proper timing between the 0 trigger and the reply signals,

(b) *Pass/inlhibit operation* (fig. FO-3 sh 4). The REPLIES GATING PASS switches S13/S14, and INHIB switches S15/S16 can be set to pass and inhibit up to 99 consecutive replies. Assuming the PASS switches are set to 30 and INHIB switches to 50, the test set generates 30 consecutive replies (one for each prt), then inhibits 50 consecutive replies (one for each prt), and so on. In operation, pass flip-flop A4U3A is in a reset state, enabling end of pass count gate A4U12A, and inhibiting end of inhibit count gate A4U12C. For each prt, a 0 trigger is generated, clocking and advancing gating counter A4U1/U2. The gating counter outputs are applied to gating pass comparator A4U7/U8, and gating inhibit comparator A4U9/U10. When the counter output reaches the selected pass count, the gating pass comparator output goes high and triggers pass/inhibit one-shot A4U13, The pass/inhibit output goes low, clearing the gating counter. When the one-shot times out, the trailing edge of the pass/inhibit output clocks and sets the pass flip-flop. Gates A4U5C and A4U12A are now inhibited and gate A4U12C is enabled. The gating counter is again clocked and advanced on count for each prt. When the selected inhibit count is reached, the gating inhibit comparator output goes high and the end of inhibit signal triggers the pass/inhibit one-shot A4U13 through end of inhibit gate A4U12C. The gating counter is cleared, and when the one-shot times out, pass flip-flop is clocked and reset, Gate A4U12C is inhibited, and gates A4U12A and A4U5C are enabled. The pass sequence is repeated as previously described, followed by the inhibit sequence, and so on. If the INHIB switches are set to zero, the output of inhibit *zero* sensing gates A4U11/U6B go low, holding the pass flip-flop in a reset state, permitting the replies to be continuously generated.

(2) *internal trigger without decode enabled (mode 4)* (fig. FO-3, sh 1). The prt counter A1U4/1J8 operates as previously described for SIF. As the prt counter advances, the decimal coded timing outputs of BCD to decimal decoders 1A1U12, U14, U16, and U18 are applied to mode 4 trigger decoding gates Al U22A/U20A. When the prt counter reaches the mode 4 delay established by the settings of switches A1S2 and S3, decode gate A1U22A outputs the mode 4 gate signal at the selected time delay. Adjustment of S2 and S3 sets the delay from 0 trigger to mode 4 gate signal in 1 µsec/ steps from 2 to 34 µsec. S1 controls the phase of the M4 clock ±1 µsec in 0.1 µsec steps. The M4 gate output of A1U22A is used to set the latch circuit consisting of A2U3D/U3C, thereby enabling the mode 4 counter chain A2U4/U5/U6. These three decade counters operate at the 1 MHz rate established by the M4 clock (from A1U20A). The BCD output of these counters drive the inputs of the BCD to decimal decoders A2U7/U8/U9. Selected outputs of A2U7/U8/U9 are decoded by a series of decode gates, A2U10A, B, C, U1lA, and U1lC to form timing triggers for mode 4 interrogation and reply signals. A2U10A, B and C decode triggers 168 µsec/ 176 µsec/ and 242 µsec after the mode 4 internal reference. These trigger times denote the start, the ISLS position, and the stop of the mode 4 interrogation signal, and are used in subsequent circuitry to generate this mode 4 pulse train. A2U11A decodes a trigger 372 µsec after the M4 internal ref and is used to generate the M4 gtc pulse at this time position (fig. FO–3, sh 2), A2U11C decodes a trigger 434 µsec after the M4 internal reference. This pulse drives delay one shot A2U13A (approx 0.5 µsec delay). This trigger is reformed by one-shot A2U13B and the output is used as a mode 4 reply trigger, driving gate A2U23C. When either M4–1P or M4–3P positions are selected on REPLIES MODULATION SEL switch S20, the mode 4 sel signal from A5U11C is high, and mode 4 replies signal from A2U13B is coupled through A2U23C and A2U18C to the reply trig signal line. When the REPLIES MODULATION SEL switch is set for any of the SIF modes (SIF, I/P MI, I/P M2/3, EMER, or GARBLE), gate A2U23C is inhibited. When the sif signal from A5U6D is high, the sif reply trig signal from A2U20B is coupled through A2U23D and A2U18C to the reply trig signal line.

(3) *Internal trigger with decode enabled* (fig. FO–3, sh 3). When TRIG SEL DCD MODE SEL switch S27 (fig. FO–19), sh 3) is placed in any position except OFF (1, 2, 3, 4, or C), both the mode 4 sel and sif select signals go low and inhibit the M4 reply (A2U23C) or the sif reply trig (A2U23D) signals from generating the reply trig signal. The decode enable signal goes through A2U25D and turns on gate A2U23B permitting decode triggers from A5U3A (fig. FO–15, sh 2) to be coupled through A2U23B and U18C to the reply trig signal line. Therefore, any replies generated by the test set are the result of challenge decodes and are not triggered from the PRT generator Section.

b. INT/DCD/EXT Operation. When S24 is in the INT position, A2U24A input is low and A2U25C input is high making the input to A2U24C low therefore, decode triggers from A2U23B are inhibited from passing A2U24C and can not be used as an enable trig signal. When S24 is in the EXT position, A2U24A input is low (same as above). Also, A2U25B input is low enabling A2U24D, allowing E trig signal to couple

through A2U24D and A2U24B to A2U25A, to become the enable trig signal. The source of the E trig signal is the signal applied to the TRIG SEL EXT TRIG IN jack of the test set (fig. FO–15, sh 2). The TRIG SEL EXT TRIG IN input is connected to a Zenner diode pulse limited on front panel board TB1. The limiter input trigger goes to A9Q5, Q6, U12A, U12B, and U6B where it is synchronized with the test set 10 MHz clock 12 signal and is provided as a buffered E trig signal through A9U2C. When S24 is in the DCD position, both inputs to A2U24A are high and the low output is inverted by A2U25C to enable A2U24C. For this condition a decode trigger passes through gate A2U23B, A2U25E, and A2U24C, A2U24B and A2U25A to become an enable trig signal. Either an external trigger applied to TRIG SEL EXT TRIG IN jack J5 (E trig signal) or a decode trigger can be the enable trig signal. The enable trig signal goes to the Al board and is used to trigger the zero trigger one-shot A1U11 for DCD or EXT operation.

c. Self Check (Internal Trigger With Decode Enabled) (fig. FO–15 and *FO–4.* Pressing BIT (MOM) switch S37 (fig. FO–15, sh 1) when DCD MODE SEL switch S27 (fig. FO– 15, sh 2) is set to any of the SIF modes or mode 4, enables gates A5U2A/U2D to transmit an sif chal trig signal or mode 4 video signal to decode shift register A5U7, U8, and U9. Pressing BIT (MOM) switch S37 also inhibits A3U6A which inhibits mode 4 challenge video to be generated. The BIT (MOM) switch also enables the 1030 MHz self test oscillator on A15. A jumper inserted between LOW PWR IN jack J1 and SUM RF IN/OUT jack J2 is used only for self-test of the rf circuits.

2-14. Output Trigger Generator (fig. FO-4)

a. The output trigger generator develops the signals available at the RDR TRIG OUT, MEASUREMENT SCOPE TRIG OUT, SIF CHAL VID PRE TRIG OUT, SIF CHAL VID OUT, MODE 4 GTC TRIG OUT, and MODE 4 CHAL VID OUT jacks. Timing for these signals is referenced to signals from the prt generator as described in paragraph 2–13. In swept rf operation, the output trigger generator also generates the sweep start triggers.

b. When the O trigger signal is generated, one-shot A3U7B is triggered, generating a signal at the RDR TRIG OUT jack through drivers A3Q13/Q14. The output of one-shot A3U7B also triggers flip-flop A3U5A/U5C. The signal at MODE 4 CHAL VID OUT jack is generated when an M4 start signal resets A3U5A/U5C. The output of A3U4A/U5C enables gate A3U5B and the 500 KHz M4 chal clk pulses are gated through. Just before the fifth pulse, the M4 isls gate signal goes high and inhibits the clock for the fifth pulse position of the train, which corresponds to the ISLS pulse. The M4 isls gate signal then goes low to continue the train of pulses. After 37 pulses have occured, the M4 stop signal sets flip-flop A3U5A/U5C, inhibiting gate A3U5B. Should a 0 trigger occur during the generation of the mode 4 video signal (because of improper setting on the PRT switches), one-shot A3U7B is triggered, and flip-flop A3U5A/U5C is set, interrupting the challenge generation. The output of gate A3U5B triggers one-shot A3U6A. One-shot A3U6A shapes to 0.5 µsec each output pulse which is amplified by A3Q9/QIO and appears at MODE 4 CHAL VID OUT jack Jll at 5 volts across 90 ohms. The signal at the MODE 4 GTC TRIG OUT jack is generated in response to a M4 GTC signal from the prt generator. The M4 GTC signal triggers one-shot A3U7A which shapes the output pulse to a pulse width of 1 µsec. The output of one-shot A3U7A is amplified by A3Qll/Q12 and appears at the MODE 4 GTC TRIG OUT jack J15 at 5 volts across 90 ohms. When SIG GEN FUNCTION switch S23 is set to FIXED FREQ gate A3U1A is enabled. When the 0 trigger triggers A3U7B its output triggers one-shot A3U3B, through inverter U4C, enabled gate U1A and U2B. The output of one-shot A3U3B is amplified by A3Q1/Q2 and appears at MEASUREMENT SCOPE TRIG OUT jack J3 at essentially 0 trigger time.

c. When SIG GEN FUNCTION switch S23 is set to either SWP ±5 MHZ or SWP ±15 MHZ gate A3U1A is inhibited; gate A3UlB is enabled when the clock signal is high (not sweeping). Triggers from A3U7B are coupled through A3U1B to trigger frequency measurement delay one-shot Q3/Q7. Period of Q3/Q7 is from 10 to 10,000 µsec selected by the front panel control MEASUREMENT FREQ MEAS. When the Q3/Q7 one-shot times out, the trailing edge is used to fire trigger one-shot A3U3A (U3A Q output is used as the sweep start signal) to start the ramp generation in the RF generator section. A3U3A Q output is used to trigger U3B to provide a sweep scope trigger.

2-15. Reply Video Generator (fig. FO-5)

The reply generator develops SIF or mode 4 reply video pulse trains in response to the delayed reply trigger and control signals from the prt generator. The reply video modulates the outputs of the rf signal generator and is also available at REPLY VID OUT jack J6 as 5 volt video at 75 ohm. The following is a general description of the reply generator operation followed by a detailed description of its major functions.

a. ***SIF OPERATION*** (fig. FO–5). When REPLIES MODULATION SEL switch S20 is set to SIF, I/P Ml, I/P M2/3A, EMERG, or GARBLE, the pulse position shift register is enabled to provide a 1.45 µsec timing cycle for the SIF reply. The $\overline{0}$ trigger clears the pulse position shift register, and on receipt of the delayed

reply trigger the pulse position shift register generates SIF 0 clock and SIF shift clock signals. Substitute (sub) pulse tap and sliding trigger tap outputs corresponding to fixed positions of REPLIES SUB PULSE POS SELECT switch S22 are also generated for each pulse position within the train. The clears the SIF coder shift register and operation is initiated by the delayed reply trigger. Each SIF shift clock pulse shifts the register input to the next location. Normal SIF and sub pulse tap outputs are generated for each pulse position in the SIF reply train. Each selected pulse in the SIF reply train, as enabled by REPLIES SIF REPLY CODE switches S1 through S4, is generated by the SIF information pulse coder logic in either the sub pulse position generator, or the sub pulse sliding position generator. The position of REPLIES SUB PULSE SEL switch S19, determines which SIF pulse in the train is used as a substitute pulse. With REPLIES SUB PULSE SEL switch S19 set to OFF, all SIF pulse train triggers (bracket, SPI, and information) are developed by the SIF information pulse coder logic using the normal SIF tap outputs from the SIF coder shift register. During emergency operation the SIF information pulse enable signal inhibits the SIF information triggers during the second through fourth pulse trains and only the bracket triggers are generated. The outputs of the SIF information pulse coder logic are ORed in the reply gating logic and trigger the reply video drivers. The reply video drivers establish the selected pulse width and apply buffered video to REPLY VID OUT jack J6 and sum and difference modulation signals to the rf signal generator. Pulse widths may be selected by REPLIES PULSE WIDTH SELECT switch S18 or continuously variable over the range of less than 0.15 to more than 1.5 µsec by REPLIES PULSE WIDTH VARY control R1A/R1B. When REPLIES SUB PULSE SEL switch S19 is set for a substitution pulse and REPLIES SUB PULSE POS SELECT switch S22 is set to a position other than 0, (-.50, -.35, etc) all the pulses of the SIF train, except the pulse to be displaced, are generated as described previously. The SIF coder shift register sub pulse tap outputs are applied to the SIF sub pulse gates and generate an SIF early sub gate signal which occurs 1.45 µsec ahead of the position corresponding to the pulse to be substituted, The early SIF sub gate signal is delayed by the M4 jamming in SIF logic and becomes the SIF sub pulse enable signal. The M4 jamming in SIF logic develops a sliding garble pulse 17.4 µsec and a fixed garble pulse 20.3 µsec/ after the selected SIF sub pulse enable signal, which is applied to the sub pulse position and sliding position generators. These generate the garble pulse trigger when the REPLIES MODULATION SEL switch is set to GARBLE. Upon receipt of the SIF sub pulse enable signal, the sub pulse position generator develops an SIF trigger concurrent with the sub pulse tap signal selected by REPLIES SUB PULSE POS SELECT switch S22. The SIF sub pulse enable signal also inhibits the normal pulse outputs of the SIF information pulse coder logic. When REPLIES MODULATION SEL switch S20 is set to GARBLE, the fixed garble signal from the M4 jamming in SIF logic triggers a second SIF sub trigger which is delayed 20.3 µsec from the selected SUB pulse in the SIF train. When REPLIES SUB PULSE POS SELECT switch S22 is set to VARY, the sliding trigger tap output, as enabled by the SIF early sub gate signal, triggers the sub pulse sliding position generator. The position of the substitute pulse is controlled by REPLIES SUB PULSE POS VARY control R2. When the sub pulse sliding position generator times out, a sliding trigger pulse is generated and triggers the reply video drivers. This permits the selected sub pulse to be continuously varied about its nominal position by ±0.8 µsec. When REPLIES MODULATION SEL switch S20 is set to 30 KHz, the 500 KHz clock signal is divided by 16 and used to drive the reply video drivers at a 30 KHz rate. When REPLIES MODULATION SEL switch S20 is set to CW, the modulation outputs of the reply video drivers are latched at a high logic level, and the rf signal generator generates continuous rf.

(1) *Pulse position shift register (fig. FO-6).* When REPLIES MODULATION SEL switch S20 is set to SIF, I/P Ml, I/P M2/3, EMERG, or GARBLE, the SIF enable signal goes high and enables gate A7U3C.

(a) The bit locations of pulse position shift register A7U4–U9 are 0.05 µsec apart, but only the tapped locations are shown on figure FO–6. When a 0 trigger is generated, the 0 trigger signal goes low, resetting register clear flip-flops A7U2A/B, which clears the register. On receipt of the delayed reply trigger, the register clear flip-flop is set and latched, removing the clear input from the register until the next 0 trigger is generated. As all inputs to gates A7U3A and A7U3C are not high at this time, the outputs of both gates are high. A high input is therefore applied to the register. On the next clock, a 1 is entered into the first bit location, and on each subsequent clock, 1's are entered into each bit location until the initial 1 is shifted into the 0.75 µsec bit location. At this time, all inputs to gate A7U3C are high and the register input goes low. On the next clock a 0 is entered into the first bit location and on subsequent clocks 0's are entered into each bit location until the initial 0 is shifted into the 0.7 µsec bit location. At this time, the 0.7 µsec input to gate A7U3C goes low and the register input goes high. A 1 is again entered into the first bit location and the cycle is repeated. This results in a 1.45 µsec timing signal which is shifted through the register and tapped off at different

points for timing purposes.

(b) The l.l µsec output provides a l.45 µsec sif shift clock signal which is applied through driver A7U10E/F to the SIF coder shift register and the M4 jamming in SIF operation.

(c) The 0.5, 0,6, 0.65, 0.75, 0.8, and 0.95 µsec outputs are sliding trigger tap signals applied to the sub pulse sliding position generator.

(d) The 1.2,1.35,1.4,1.45,1.55, 1.65,1.75,1.85, 1.95,2.15, 2.2, 2.25, and 2.4 µsec outputs are sub pulse taps applied to the sub pulse fixed position generator.

(e) The 1.9 and inverted 2.05 µsec outputs are combined at gate A7UlD/U21 B, for form the 0.15 µsec SIF 0 clock pulse which applied to the SIF information pulse coder logic to clock out the selected pulses.

(2) *SIF coder shijt register logic* (fig. FO–7). The generation of the O trigger clears the SIF coder shift register and the delayed reply trigger initiates the register operation. The reply trigger bit entered into the register is shifted one bit position for each sif shift clock signal, providing separate outputs corresponding to the pulse positions of the SIF reply train. These are gated out through the SIF information pulse coder logic. For mode 1 –I/P and emergency operation, the register repeats the shift cycle once for the mode 1 –I/P operation, and three times for emergency operation. In the emergency mode, the information pulses are inhibited at the output so that only one reply train plus three sets of bracket pulses are generated. The SIF reply format and information pulse combinations for the various types of operations are shown in figure 2– 10. At the start of each PRT cycle, the 0 trigger is generated, and the 0 trigger signal goes low clearing SIF coder shift register A8U4/U9/U13 and cycle counter flip-flops A8U19A/U19B. SIF information pulse enable gate U15A is activated and the SIF information pulse enable signal at the output of U2B goes high. When the delayed reply trigger is generated, the delayed reply trigger signal goes low, setting register enable flip-flop A8U3C/U1B. On the next pulse of the 1.45 µsec SIF shift clock pulse, a 1 is entered into the first bit location of the ‘register. Output F1 goes high, resetting the register enable flip-flop A8U3C/UlB. Each subsequent SIF shift clock pulse shifts the 1 through the register bit locations. The 1 appears sequentially at each of the register outputs generating the SIF and sub pulse tap signal position gates. The SIF tap outputs are applied to the SIF information pulse coder logic, generating the SIF information triggers to the reply gating logic. Cycle counter flip-flop A8U19A is clocked and set when the 1 is shifted out of the 23.2 µsec position. This completes the SIF coder operation when REPLIES MODULATION SEL switch S20 is initially set to SIF, I/P M2/3, or GARBLE. When the REPLIES MODULATION SEL switch is set to I/P Ml, mode 1 I/P register gate A8UIA is enabled, through inverter A8U14D and SIF information pulse enable gate U15B is activated. The reply code is generated as previously described. When the 23.2 µsec output goes high, gate output Ml I/P restart goes low, setting the register enable flip-flop. On the next SIF shift clock pulse a second 1 is entered into the register and cycle counter flip-flop A8U19A is set, inhibiting gate U1A. The second reply train following the first by 4.35 µsec is generated to complete the operation. If the REPLIES MODULATION SEL switch is set to EMERG, emergency register gate U16A is enabled, through inverter A8U14C. When the 23.2 µsec output goes high at the end of the first cycle, gate output emergency goes low, setting the register enable flip-flop. The cycle counter is clocked, disabling SIF information pulse enable gate U15A. The SIF information pulse enable signal goes low, inhibiting the SIF information pulses for the next three cycles, At the end of the second cycle, the register enable flip-flop is set and the cycle counter clocked. At the end of the third cycle, the register enable flip-flop is set and the cycle counter is clocked, activating gate U3B which disables emergency register gate U16A, The emergency signal goes high, and at the end of the fourth cycle, the register enable flip-flop cannot be set. This completes the emergency operation.

(3) *SIF information pulse coder logic* (fig. FO–7), The individual SIF information pulses are gated through the applicable gates enabled by REPLIES SIF REPLY CODE switches S1 through S4. In SIF operation, the SIF sub pulse enable signal is low, enabling gate A8U17A. The selected SIF information pulses are gated through A8U17A by the SIF 0 clock pulse. The F1 and F2 bracket pulses and the SPI pulse in I/P M2/3 operation are gated through A8U16B by the sif 0 clock pulses. When REPLIES MODULATION SEL switch S20 is set to EMERG, the information pulses are gated out for the first SIF coder shift register cycle as previously described. The sif information pulse enable signal then goes low, inhibiting gate A8U17A. Therefore, only the F1 and F2 bracket pulses are gated through A8U16B for the next three register cycles. Thus the emergency reply is one SIF pulse train followed by three sets of bracket pulses.

(4) *Reply gating logic* (fig. FO–7). When generated, the sif bracket and spi triggers, sif information and sub triggers, the M4 reply and sub triggers, and the gated M4 jamming trigger are ORed through A8U17B, triggering reply trigger generator one-shot A8U20. The reply trig signal output is applied to the pulse width generator one-shot A9U1/U3/U4C (FO-11) and ORed through A9U5B and to drivers A9Q3/Q4 to provide the REPLY VID OUT signal. The output of A9U5B also provides the

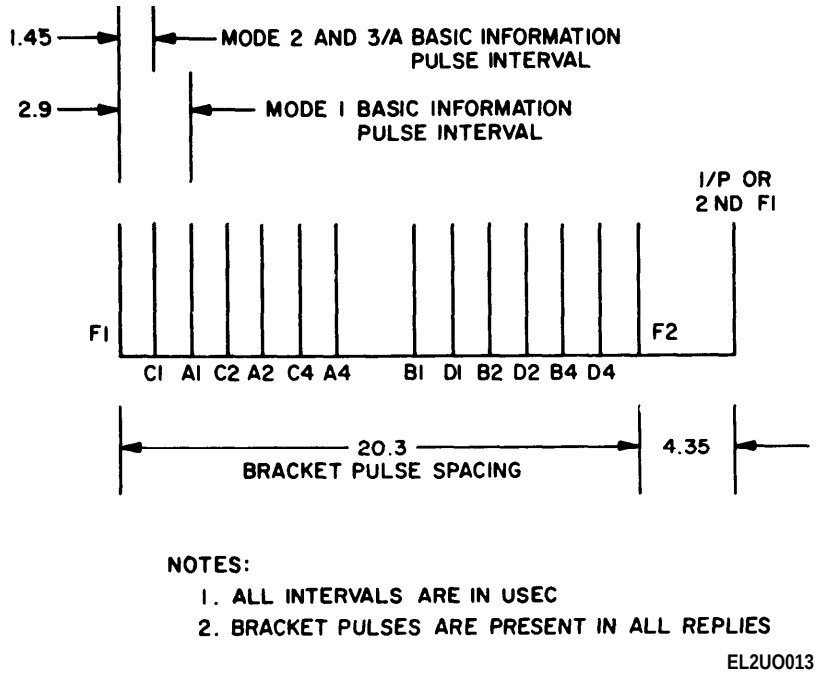

Figure 2-10. Typical SIF reply trains.

modulation pulses for the rf output,

(5) *SIF sub puke gates* (fig. FO-8 and FO- 13). The pulse to be substituted is enabled by REPLIES SIF REPLY CODE switches S1 through S4 and selected with REPLIES SUB PULSE SEL switch S19. When a substitute pulse is selected, the information pulse gate, which occurs 1.45 µsec ahead of the pulse gate to be substituted, is gated through the selected SIF sub pulse gate as the sif early sub gate signal.

(6) J41 *jamming in SIF logic.* The M4 jamming in SIF logic develops the sub pulse enable, sliding garble enable, and fixed garble enable signals. Setting REPLIES MODULATION SEL switch S20 to any SIF position provides an SIF enable signal which enables the M4 jamming in SIF logic for SIF operation. The 0 trigger signal initially clears M4 jamming shift register A6U2/U6. The sif shift clock signal then shifts the M4 jamming shift register, The sif early sub gate signal goes high and sets register enable flip-flop A6U4B/U5A. The SIF shift clock pulse enters a 1 into the M4 jamming shift register, and shifts it through, generating a 1.45 µsec sif sub pulse enable output. The SIF sub pulse enable signal resets the register enable flip-flop through A6U7A, enables the generation of the substitute pulse by the sub pulse position generator, and inhibits the generation of the normal information pulse from the SIF coder. If REPLIES MODULATION SEL switch S20 is set to EMERG, a subsequent substitute kill (ssk) signal is developed to inhibit the substitute pulses occurring during the three sets of added brackets for emergency operation.

(7) *Sub pulse fixed position generator* (fig. FO-9), The sub pulse fixed position generator displaces the substitute pulse from its nominal position in the reply pulse train by the amount selected by REPLIES SUB PULSE POS SELECT switch S22. If the REPLIES SUB PULSE POS SELECT switch S22 is set to VARY or 0, or REPLIES SUB PULSE SEL switch S19 is set to OFF, the inhibit sub pulse output of gate A7U16A/U19A goes low, disabling gate A7U22C and inhibiting the operation of the sub pulse position multiplexer A7U23/U24. For SIF and mode 4–P2 substitution, the settings of REPLIES MODULATION SEL switch S20, and the REPLIES SUB PULSE SEL switch S19 enable SIF and M4–P2 multiplexer A7U23. For mode 4 – P3 substitution the settings of these switches also enable M4 –P3 multiplexer A7U24. The position of the substitute pulse in the reply train relative to the nominal position of the normal information pulse is determined by the REPLIES SUB PULSE POS SELECT switch S22 and the sub triggers developed from the multiplexer outputs. The REPLIES SUB PULSE POS SELECT switch S22 provides a BCD coded signal for each switch position which corresponds to an input line of the SIF and M4–P2, and M4–P3 multiplexer. The sub pulse tap from the pulse position shift register, which is on the selected input line, is gated to the out-

put of the multiplexer. In SIF operation the output of gate A7U22C is low, enabling the SIF and M4–P2 multiplexer, and the output of gate A7U22A is high, inhibiting the M4–P3 multiplexer. When REPLIES SUB PULSE POS SELECT switch S22 is set to -.25, a BCD count of 2 is applied to the select inputs of the SIF and M4-P2 multiplexer, and input 1.65 is enabled to the multiplexer output. The 1.65 µsec sub pulse tap signal is gated to the multiplexer output and applied to delay A7U25A/B/C and gate A7U26A. The delay ensures that the M4–P2 and SIF sub trigger pulse is approximately 100 nsec wide. The multiplexer taps on A7U23 are referenced to a 1.9 µsec offset for a pulse in the normal position. The corresponding pulse position to multiplexer tap relationships are as follows:

Tap				*S22 Switch Position*
2.4	-	1.9	=	+.50
2.25	-	1.9	=	+ .35
2.15	-	1.9	=	+ .25
2.05	-	1.9	=	+.15
1.75	-	1.9	=	-.15
1.65	-	1.9	=	-.25
1.55	-	1.9	=	-.35
1.4	-	1.9	=	-.50

In the emergency operation, the ssk signal goes low inhibiting gate A7U26A and the output of any sub pulses during generation of the three empty sets of the emergency pulse train. When REPLIES MODULATION SEL switch S20 is set to GARBLE, a second SIF sub trigger pulse is produced when the sub pulse tap output and the fixed garble enable signal are coincident at gate A7U26A. When REPLIES MODULATION SEL switch S20 is set to M4–3P and REPLIES SUB PULSE SEL switch S19 is set to M4 - P2, the SIF and M4 – P2 multiplexer operates as described previously to develop the P2 substitute pulse. When the P2 pulse of the mode 4 reply is generated, sub pulse tap 1.9 goes high. The output of gate A7U20B goes low, triggering mode 4–P3 sub position stretch one-shot A7U18B. The M4–P3 sub one-shot signal is applied to gate A7U10B/UllD and M4–P3 multiplexer A7U24 is enabled. The M4-P3 sub one-shot output is also applied to the mode 4 fixed target generator and enables the displacement of the P3 substitute pulse to its maximum limits. The selected sub pulse tap signal is gated to the output of the multiplexer and applied to gate A7U26B and delay A7U25D/E/F, The delay ensures that the M4–P3 sub trigger pulse is approximately 100 µsec wide. The multiplexer taps on A7U24 are referenced to an offset for a pulse in the normal position. The corresponding pulse position to multiplexer tap relationship are as follows:

Tap			*S22 Switch Position*
2.2	1.7	=	+.50
2.05	1.7	=	+.35
1.95	1.7	=	+ .25
1.85	1.7	=	+.15
1.55	1.7	=	-.15
1.45	1.7	=	-.25
1.35	1.7	=	-.35
1.2	1.7	=	-.50

(8) *Sub pulse sliding position generator* (fig. FO–10). Setting REPLIES SUB PULSE POS SELECT switch S22 to VARY enables the sub pulse sliding position generator. In the SIF modes of operation the SIF early sub gate and gated BK–2 signals enable gate A6U15B. When the 0.5 sliding trigger tap is high and the 0.65 sliding trigger tap is low, gate A6U15B is activated, and the output of gate A6U16B triggers sliding sub pulse one-shot U17. The duration of one-shot A6U17 is controlled by REPLIES SUB PULSE POS VARY control R2. When one-shot A6U17 times out it triggers sliding sub pulse shaper one-shot A6U18A which generates the sliding trigger signal. If REPLIES MODULATION SEL switch S20 is set to GARBLE, the sliding garble enable signal enables gate A6U15B. This signal occurs 20.3 µsec after the first triggering of sliding sub pulse one-shot A6U18. The one-shot is again triggered and a garble pulse sliding trigger is generated. In mode 4 3-pulse reply operation, M4–P2 sub gate A6UlA/U14B is enabled when REPLIES SUB PULSE SEL switch S19 is set to M4-P2. The sliding trigger signal is generated when the 0.8 sliding trigger tap is high and the 0.95 sliding trigger tap is low. If REPLIES MODULATION SEL switch S20 is set to M4–lP, the M4–P2 sub gate is inhibited and the P2 sub pulse cannot be generated. In mode 4 reply operation, setting REPLIES SUB PULSE SEL switch S19 to

M4–P3 enables M4–P3 sub gate A6U15A/U12F. The sliding trigger signal is now generated when the 0.75 sliding trigger tap is high and the 0.6 sliding trigger tap is low.

(9) *Reply video drivers* (fig. FO–11). The reply video drivers establish the reply pulse width of the sum and difference modulation video outputs and the pulse at REPLY VID OUT jack J6. The REPLY VID OUT pulse width is selected by the REPLIES REPLY WIDTH switch S18 as 0.90, 0.50, 0.45, or 0.15 µsec or variable from 0.15 µsec to 1.5 µsec. The REPLY VID OUT jack provides a 5 volt output into a 75 ohm load. The reply video drivers also provide compensation for pulse width differences between the RF and video outputs. The 30 KHz counter A9Ull/U5A generates output pulses at a 30 KHz rate when REPLIES MODULATION SEL switch S20 is set to 30 KHZ. The reply trig signal triggers pulse width generator one-shot A9U1/U3/U4C.

The output duration of the pulse width generator one-shot is controlled by REPLIES REPLY WIDTH switch S18. The one-shot output triggers pulse width adjust circuit A9U8C/DLl/U9C, and is also normally applied to the REPLY VID OUT jack J6. The output of pulse width adjust circuit is shown applied to the rf signal generator, and compensates for a difference in pulse widths between the video at the REPLY VID OUT jack and the modulated rf outputs. Without compensation, the width of the pulse at the REPLY VID OUT jack J6 may be wider or narrower than the reply rf pulses at the RF IN/OUT jacks. Trim adjust switch S1 compensates for the characteristics of the test set. Output connections are made with jumpers on terminals El thru E4. As indicated by the dashed lines in figure FO–11, the outputs of gate A9U5B and pulse width adjust circuit A9U8C/DLl/U9C, can be switched if required. Output connections are switched, if the characteristics of the test set are such that the pulses of the REPLY VID OUT jack J6 are narrower than the reply rf pulses. With SIG GEN NORM/INTERLEAVE switch S36 set to NORM, gate A9U9B is enabled, and gate A9U8B/U10A is inhibited. The sum modulation video pulse then generates a difference modulation video pulse through gates A9U9B and A9U9D/U10F/U10E. If the SIG GEN NORM/INTERLEAVE switch is set to INTERLEAVE, gate U9B is now inhibited and A9U8B/U10A is enabled. The sum modulation video pulse now generates the difference modulation video pulse through gates A9U8B/UIOA, delay A9DL2/3/4, and gate A9U9D/U10F/U10E. This delays the difference modulation video pulse 0.7 µsec from the sum modulation video pulse. The sum and difference modulation video signals are then combined in the rf signal generator as one rf output. Delay adjust switch S2 sets the delay between the sum and difference modulation video signals. When REPLIES MODULATION SEL switch S20 is set to CW the output of gate A9U9A/U10D is latched high and a continuous rf output is generated. When REPLIES MODULATION SEL switch S20 is set to 30 KHZ, gate U4D is enabled. When the 0 trigger is initially generated, the 0 trigger signal goes low, resetting 30 KHz ripple counter U1l/U5A. When the 0 trigger goes high, the counter is enabled and the 500 KHz input signal is divided by 16 to develop approximately 30 KHz. This triggers pulse width generator one-shot U1/U3/U4C at the 30 KHz rate. The sum and difference modulation video pulses modulate the rf output at the same rate. In the substitute pulse operation, if a sliding trigger pulse is generated, it triggers sliding pulse generator one-shot A9U7. The sliding pulse is generated separately from the reply trigger signal to provide proper pulse operation regardless of positioning of the substitute pulse within the reply train. The A9U7 one-shot output is ORed to the basic modulation signal by A9U5B. If REPLIES MODULATION SEL switch S20 is set to OFF the pulse width and sliding pulse generator one-shots are disabled, and all replies are inhibited. The pass/inhibit signal, modulation blanking between sweeps, the ext gate in signal and the PRT/overlap sensor blanking all can cause a blanking and replies off signal to be generated. Under this condition one-shot A9U1/U3/U4C and one-shot U7 are inhibited, and all replies are inhibited.

b. Mode 4 Operation (fig. FO–5, FO–6, FO–12, and FO-13). When REPLIES MODULATION SEL switch S20 is set to M4–lP or M4–3P, the test set generates a corresponding l-pulse or 3-pulse reply. The pulse position shift register is cleared by the 0 trigger signal, and the mode 4 reply cycle begins on receipt of a delayed reply trigger. The pulse position shift register is clocked by the 20 MHz clock signal and generates a M4 shift clock signal every 40 µsec. The M4 tap outputs establish the mode 4 reply pulse intervals for both the normal and jamming triggers which are generated by the M4 jamming trigger generator. The M4 jamming in M4 logic generates gated M4 jamming triggers controlled by REPLIES M4 JAMMING switch S17 and the M4 fixed trigger signal which occurs 60 µsec after the start of the M4 shift clock. The M4 fixed trigger signal also enables the mode 4 fixed target generator and the M4 tap inputs to generate M4 fixed target trigger outputs. The M4 fixed target trigger signals are ORed in the reply gating logic, and applied to the reply video drivers which operate as previously described. When REPLIES SUB PULSE SEL switch S19 is set to M4–P3 or M4–P2 the sub pulse position or sliding position generator generates the M4 – P2 or P3 substitute triggers as described previously for SIF operation.

(1) *Pulse position shift register* (fig. FO-6). For

mode 4 operation, REPLIES MODULATION SEL switch S20 is set to M4–3P or M4–1P. In these positions, the mode 4 enable signal goes high, enabling gate A7U3A. The register clear flip-flop is set and latched by the delayed reply trigger and 1's are clocked into the register as previously described. For mode 4 operation, a 4 µsec time base signal is developed by the register, This timing is determined by a trigger from the 2.0 µsec tap. When the 2.0 µsec tap goes high, gate A7U3A is activated and 0's are entered into the register for 2 µsec. The cycle is continually repeated and a 4 µsec mode 4 shift clock signal is applied to the M4 jamming in M4 logic. The 0.1, 0.3, 1.7, 1.8, 1.9, and 2.05 µsec outputs are M4 tap signals applied to the M4 jamming trigger generator and mode 4 fixed target generator.

(2) *Mode 4* fixed *target generator* (fig. FO-12). The mode 4 fixed target generator is enabled when REPLIES MODULATION SEL switch S20 is set to M4–3P or M4–1P, and REPLIES SUB PULSE SEL switch S19 is set to OFF. With S20 set to M4–3P, the M4FT (fixed target) signal enables M4–P1 gate A7U21A, and M4–2P gate A7U28A through gates A7U19B/U27C, U19C and U21C. When the 0.1 M4 tap is high and the 0.3 M4 tap is low, a M4–P1 pulse is gated through A7U21A, When the 1.9 M4 tap is high and the 2.05 M4 tap is low, a M4–P2 pulse is gated through A7U28A. For both 3-pulse and l-pulse reply operation, when the 1.7 M4 tap is low, and the 1.8 M4 tap is high a M4–P3 pulse is gated through gate U14A. The M4–P1, P2, and P3 pulses form the M4 fixed target trigger signal which is gated through U28B to the reply gating logic. The pulses are spaced 1.8 µsec apart, and represent a mode 4 three-pulse reply. When REPLIES SUB PULSE SEL switch S19 is set to M4–P2 and REPLIES SUB PULSE POS SEL switch S22 is set to any position but O, the M4–P2 gate A7U28A is inhibited. The M4–P1 and P3 pulses are gated out as before, and the substitute P2 pulse is generated by the sub pulse fixed position generator (fig. FO–9) as described previously. If REPLIES SUB PULSE SEL switch S19 is set to M4–P3, the M4–P3 gate A7U14A is inhibited. The M4–P1 and P3 pulses are now gated out as before, and the substitute P3 pulse is generated by the sub pulse position generator. During a mode 4 reply operation, if REPLIES SUB PULSE SEL switch S19 is set to any position other than M4–P2 or M4–P3, the M4-P2 and P3 gates are enabled through gate A7U27B and the mode 4 operation is not affected.

(3) *M4 jamming trigger generator* (fig. 2–11). During mode 4 reply operation, the M4 jamming trigger generator produces sets of jamming triggers at 4 µsec intervals. The interval timing is established by the pulse position shift register (fig. FO–6) as previously described for SIF operation, and the triggers are developed from the pulse position shift register M4 taps. When REPLIES MODULATION SEL switch S20 is set to M4-3P, a 3-pulse M4 jamming trigger is generated every 4 µsec. When REPLIES MODULATION SEL switch S20 is set to M4–1P, a single M4 jamming trigger is generated every 4 µsec. For 3-pulse reply operation, gate A7U16 is enabled when REPLIES MODULATION SEL switch S20 is set to M4-3P. The P1 pulse is gated through M4–P1 gate A7U20A when the 0.1 M4 tap is high and the 0.3 M4 tap is low. The P2 pulse is gated through M4–P2 gate A7U 20B when the 1.9 M4 tap is high and the 2.05 M4 tap is low. The P3 pulse is gated through M4–P3 gate A7U20C when the 1.7 M4 tap is low and the 1.8 M4 tap is high. The pulses are spaced 1.8 µsec apart as in a normal mode 4 reply. They are applied through gate A7U2D to the M4 jamming in M4 logic. For single pulse reply operation, gate A7U16C is inhibited when REPLIES MODULATION SEL switch S20 is set to M4–lP. Only the P3 pulse is now gated through A7U2D.

(4) *M4 jamming in M4 logic* (fig. FO–13). The M4 jamming in M4 logic develops timing for the mode 4 fixed target generator and gates the M4 jamming triggers initiated by the M4 jamming trigger generator to the reply gating logic. The gated M4 jamming triggers signal simulates a non-synchronous mode 4 reply, and up to five sets of jamming triggers can be generated for each interrogation. When the O trigger is generated, the 0 trigger signal goes low, clearing M4 jamming shift register U2/U6. On receipt of the delayed reply trigger, register enable flip-flop U4B/U5A is set. On the next M4 shift clock pulse, gated through U1A/C, a 1 is entered into M4 jamming shift register U2/U6. The 4 µsec output goes high, and resets the register enable flip-flop. The 1 is shifted through the register by subsequent clock pulses and the register provides timing outputs. Three-stage ring counter U13A/U13B/U14A/U9 D/U3D sequentially enables gates U10B, U10A, and U10C. It is clocked by the delayed reply trigger each prf. REPLIES M4 JAMMING switch S17 selects the number of jamming triggers to be generated. When the REPLIES M4 JAMMING switch S17 is set to 0, gate U7C is enabled, and the 4 µsec register output sets flip-flop U4D/U4C. Gates U10B, U10A, and U10C are inhibited for the complete cycle, and prevent any jamming outputs. At the end of the cycle the 64 µsec output goes high, generating the M4FT signal and sets flip-flop U4D/U4C for the next cycle. When REPLIES M4 JAMMING switch S17 is set to 1, gate U7D is enabled, and one gated M4 jamming trigger pulse is generated for each PRT. The jamming reply occurs at 52,56, or 60 µsec before the M4 signal as determined by the 3-stage ring counter. When the 16th output of the shift register goes high, flip-flop U4D/U4C is set inhibiting further jamming replies. Setting REPLIES M4 JAMMING switch S17 to any other position causes a

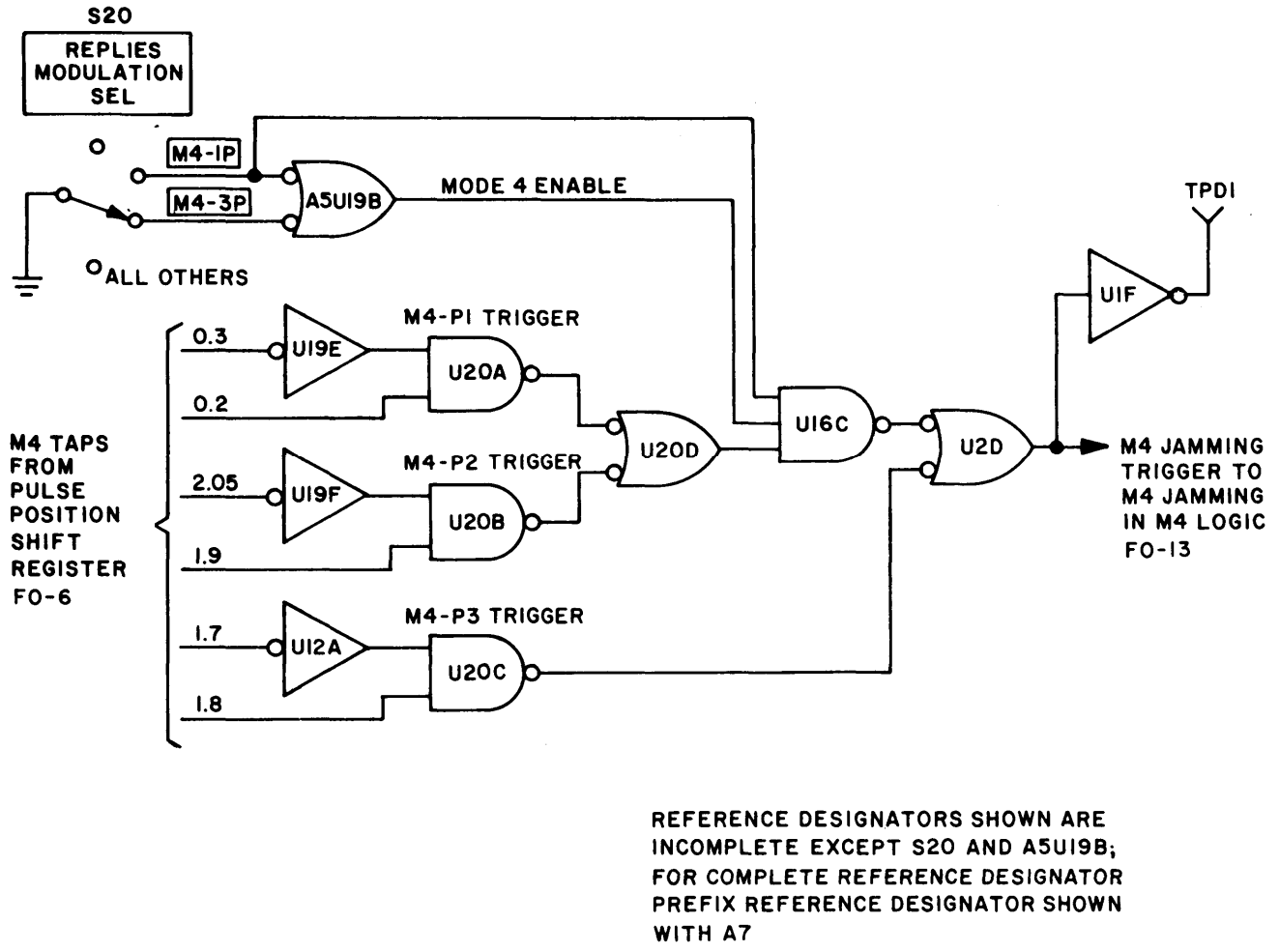

Figure 2-11. SIF and mode 4 reply generator, mode 4 jamming trigger generator, logic diagram.

corresponding number of jamming replies to be generated in the manner described.

2 – 16. Rf Signal Generator (fig. FO-14)

The following is a description of the overall rf signal generator operation. This is followed by a more detailed description of marker/ramp generator AllAl, rf source A11A2, and dual modulator A16.

a. Fixed Frequency Operation. In fixed frequency operation, a 1090 MHz cw rf signal is developed by rf source A11A2. The rf signal level is +22 dBm nominal and is applied through circulator HY3 to dual modulator A16. The sum and difference modulation video signals from the video generator modulate the sum and difference rf outputs respectively.

(1) The sum rf output from dual modulator A16 is applied through 9 dB coupler DC2, SUM ATTEN control AT1, and circulator HY3 to the SUM RF IN/OUT jack HY3J2, Coupler DC2 combines the interleave rf signal when present with the sum rf output signal. The SUM ATTEN control AT1 adjusts the rf output level from O to -90 dBm. Circulator HY3 couples an input rf signal from the SUM RF IN/OUT jack to the receiver. With the SUM ATTEN at 0 dBm, the accumulated attenuation from the rf signal generator output to the SUM RF IN/OUT jack is nominally 22 dB. The output level at the SUM RF IN/OUT jack can be adjusted to the calibrated level of the SUM ATTEN by adjusting A16A1R40.

(2) When the SIG GEN NORM/INTERLEAVE switch S36 is set to NORM the difference rf output signal from dual modulator A16 is applied through DIFF/INTERLEAVE ATTEN control AT2, energized rf switch S35, adjustable pad AT5, multi/coupler DC3, and attenuator AT4 to the DIFF RF IN/OUT jack AT4J2. The DIFF/INTERLEAVE ATTEN control adjusts the rf output level from 0 to -90 dBm. Attenuator AT5 adjusts the rf signal level 0.5 to 3.0 dB and is used to balance the sum and difference

signal paths when aligning the test set with the DIFF/INTERLEAVE ATTEN at 0 dBm. The accumulated attenuation from the rf signal generator output to the DIFF RF IN/OUT jack is nominally 22 dB. Setting the SIG GEN NORM/INTERLEAVE switch S36 to INTERLEAVE energizes switch S34 and deenergizes rf switch S35, The cliff rf output signal from dual modulator A16 is delayed 0.7 µsec from the sum rf output signal from dual modulator A16 and is routed through the rf switches and combined in coupler DC2. With the SUM ATTEN and DIFF/INTERLEAVE ATTEN at O dBm, and SIG GEN NORM/INTERLEAVE switch to INTERLEAVE, the accumulated attenuation from the rf signal generator difference output to the SUM RF IN/OUT jack is 22 dB. This output level can be adjusted by adjusting A16A1R39.

b. Swept Frequency Operation. In swept frequency operation, rf generator ***Al 1*** generates either a narrow or wide sweep rf signal and frequency markers. The rf sweep width is selected with SIG GEN FUNCTION switch **S23** and controlled by the sweep ramp output of marker/ramp generator All Al. Setting SIG GEN FUNCTION switch S23 to SWP ± 5 MHZ, generates a narrow sweep rf signal which varies from 1085 to 1095 MHZ with markers corresponding to 1025, 1029, 1030, 1031, and 1035 MHZ. Setting the switch to SWP ± 15 MHZ generates a wide sweep rf signal which varies from 1075 to 1105 MHZ, with markers corresponding to 1075, 1080, 1085, 1089, 1090, 1091, 1095, 1100 and 1105 MHZ. The sweep prf is controlled by sweep start signal from the mode 4 interface and trigger generator card A3.

2–17. Sweep Triggering

(fig. FO-4 and FO-14)

When SIG GEN FUNCTION switch S23 is set to SWP ± 5 MHZ or SWP × 15 MHZ gates A3U1B and U2A are enabled while A3U1A is inhibited. If the sweep clock sync signal is high, a O trigger signal passes through one-shot A3U7B, inverter A3U4C and gate A3U1B to trigger one-shot A3Q3/Q7. The amount of delay of A3Q3/Q7 is controlled by MEASUREMENT FREQ MEAS control R3. The output from A3Q3/Q7 triggers one-shot A3U3A and a sweep start signal is transmitted to the rf generator All. A3Q3/Q7 also triggers A3U3B through OR gate A3U2B, and the resulting trigger is buffered by A3Q1/Q2 and provided as a MEASUREMENT SCOPE TRIG signal. The MEASUREMENT SCOPE TRIG output is a 5 volt signal when loaded by 90 ohms. Upon receipt of a sweep start signal, RF signal generator A 11 provides a sweep clock sync signal which is low until approximately 400 µsec after the rf output of the test set has completed its sweep. The sweep clock sync signal is used to inhibit A3U1B so A3Q3/Q7 cannot be triggered until the sweep operation is complete. After the sweep clock sync signal goes high again, the above process is repeated upon receipt of the next O trigger signal input. A pos gate signal from the RF signal generator A11 is produced for the duration of the sweep only. During this period A3U4D goes low and causes A3U2A output to provide a blanking and replies off signal. A high blanking and replies off signal enables replies to be generated on the A9 card only for the duration of the sweep.

2-18. Ramp Generator

(fig. FO-14)

a. Marker/Ramp Generator Card A11A1, The marker/ramp generator card generates the ramp and signals when triggered by a sweep start pulse from A3. The pos gate out signal is generated by one-shot U1lB and with switch S23 in the SWP ±5 MHZ position an approximate 800 µsec signal is selected and controlled in length by resistor A11A1R79. U1lA is triggered at the conclusion of the pos gate pulse, which inhibits a retriggering of A11A1U11B for an additional 400 µsec. The pos gate signal is also used to enable ramp generator (A11A1U8, U9, U3, and Q4) providing a ramp out signal to the RF source AllA2. The slope and ramp start voltage of the ramp out signal is controlled by resistors A11A1R66, A11A1R73, and A11A1R74,

b. RF Source (fig. F0–14, and fig. 2–12 and 2–13). Rf Source A11A2 contains two phase lock loops, the primary phase lock loop A11A2A1 and the secondary phase lock loop in the power oscillator A11A2A2.

(1) *Secondary phase lock loop*. The secondary phase lock loop locks the (voltage controlled) power oscillator to the eightieth harmonic of the input signal from the primary phase lock loop. In fixed frequency operation the primary loop provides a 13.625 MHz reference signal to A11A2A2U1 phase detector. Output from the power oscillator is sampled in the directional coupler A11A2A2DC and frequency

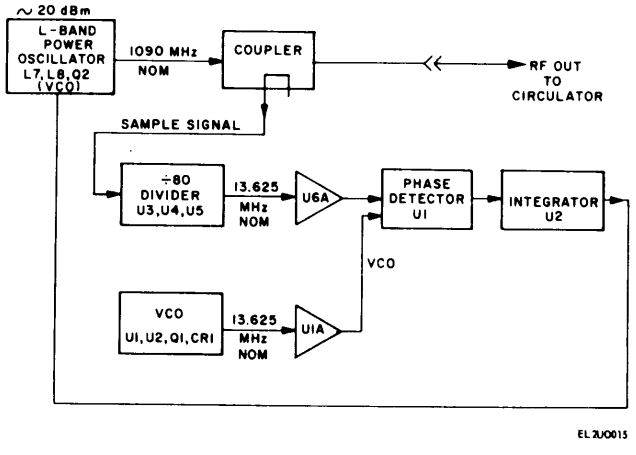

Figure 2-12. Secondary phase lock loop (A11A2A2) block diagram.

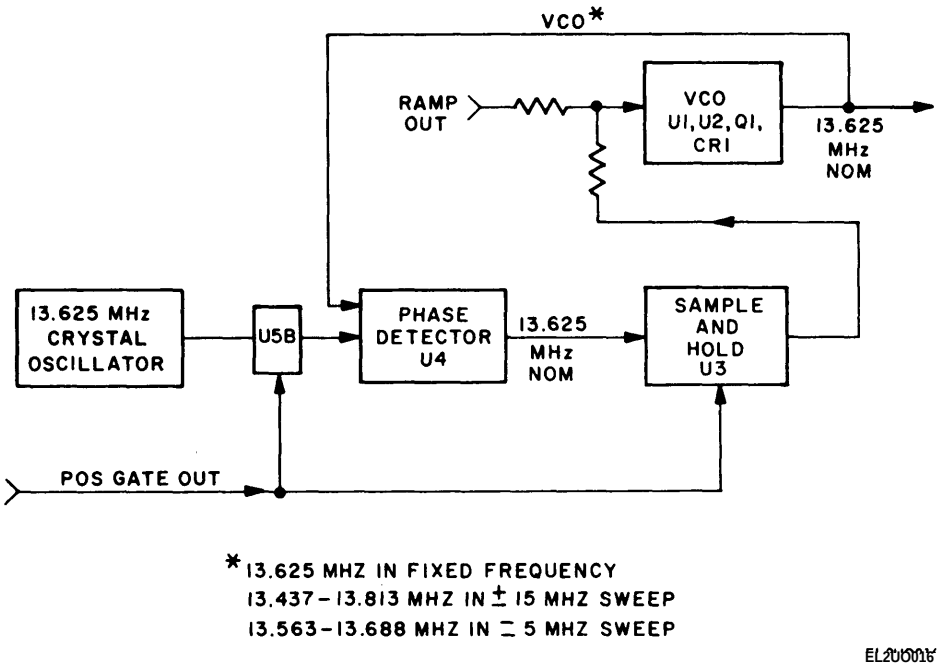

Figure 2-13. Primary phase lock loop (A11A2A1) block diagram.

divided by eighty by counter A11A2A2U3, U4 and U5. The resulting output is amplified by A11A2A2U6A and provided as a second input to phase detector Al1A2A2U1. When a difference in frequency occurs between the phase detector input signals a correction voltage is sent through integrator A11A2A2U2 to the VCO input of the power oscillator. The power oscillator frequency is corrected and phase locked to the reference signal input from the primary phase lock loop. In swept operation the primary frequency loop is swept about 13.625 MHz, The secondary phase lock loop characteristics are such that the loop remains locked to the input signal and follows the primary frequency loop output. As a result the power oscillator is swept over a range eighty times that of the input frequency.

(2) *Primary phase lock loop.* In the primary phase lock loop (primary frequency loop A11A2A1) the ramp out signal causes VCO (Ul, U2, Q1 and CR1) to sweep about 13.625 MHz, when the swept mode is selected. The pos gate signal disables the 13.625 MHz crystal controlled reference oscillator U5, Y1, and takes the sampled phase detector output from U4 and U3 and holds this voltage during the portion of the sweep cycle when the VCO is being activated by the ramp voltage. In the fixed frequency mode crystal oscillator (U5, Yl) is continuously connected to phase detector U4 which phase locks the entire system to 13.625 MHz (80th harmonic of the primary frequency, 1090 MHz).

c. *Frequeeny Marker Generation* (fig. FO – 14). The output from divide-by-80 counter A11A2A2, U3, U4 and U5 is amplified and supplied to the crystal markers A11AIY1–Y9. The crystals are selected to be f marker /80. When the power oscillator output divide-by-80 output sweeps by the frequency of the crystal, the crystal passes an output which is detected, filtered, amplified and gated. One-shot AllAlU6A/B provides a 2 µsec output to the FREQ MKRS OUT jack. A11A1U7 is triggered at the end of each sweep ramp to inhibit generation of a FREQ MKRS OUT signal during the retrace of the swept oscillator. Each marker generator has one crystal. The crystal outputs are rectified within each generator and applied to its respective threshold amplifier. Potentiometer CR6, Rll, R16, R21, R26, R31, R36, R41, and R46 establish the marker output frequency, and the markers are applied through quad line receivers A11A1U3, U4, and U5 to one-shot U6A and U6B, and the outputs are combined at the junction of CR10 and CR1l and seen at markers out jack after being isolated by emitter follower Q2.

d. Dual Modulator A16 (fig. FO–14). Dual modulator A16 contains sum and difference rf modulators. The sum modulation trigger pulse from the video generator is applied through inverter A1U1A and A1U1B to driver amplifier AlQ7/Q8, and through inverter A1U1A to driver amplifier AlQ5/Q6. The push-pull driver applied bias to the sum modulator and the rf input from rf generator Al 1 is effectively modulated by the sum modulation video. The sum modulated rf output is applied to 9 dB coupler DC2 as previously described. In the absence of a sum modulation video signal, the sum modulator

is biased-off, and there is no sum rf output. Potentiometer R40 sets the sum modulator plus voltage level applied to the output driver, The operation of the difference modulator is as described for the sum modulator. When the REPLIES MODULATION SEL switch is set to CW, the sum modulation video and difference modulation video inputs remain high holding the sum and difference modulators in the on condition. Signals applied to the EXT MOD IN jack are applied directly to the sum section of the dual modulator and the operation is the same as described previously.

2-19. Receiver

(fig. F0-15)

Inputs to the receiver (nominally 1030 MHz) are acted upon in two ways: they are detected, amplified, and applied to the measurement section, and also mixed with a local oscillator signal to produce an if signal which is amplified, detected and applied to the measurement section. In fixed frequency operation, the input signal is detected only, and measured for peak power and pulse fidelity. In swept frequency operation, the input signal is mixed, amplified, detected, and measured for frequency.

a. Video Fidelity and Peak Power Measuremen t. Signals from *40* watts to 4 KW are applied to the RF IN/OUT jacks. An rf signal applied to SUM RF IN/OUT jack HY3J2, passes through circulator HY3, which contains a 26 d B attenuator, to multicoupler DC3. An rf signal applied to DIFF RF IN/OUT jack AT4J2, passes through attenuator AT4 to multicoupler DC3. The detector amplifier AR2 is adjusted so that the output level of it is the same for rf of equal power applied to either RF IN/OUT jack. The output form detector amplifier AR2 passes through the MEASUREMENT DEMOD VID LEVEL control to the peak power video and prf card A10 as an adjusted video signal, RF signals from -12 to +3 dBm are applied to JOW PWR IN jack Jl, and coupled through multicoupler DC3 to A10Q1. A difference of 61 dB between the rf power levels applied to the RF IN/OUT jacks and LOW PWER IN jack provides the same video level input to the Al0 card. When MEASUREMENT FUNCTION SEL switch S31 is set to PRF CHAL the fidelity and power video signal is routed through video amplifier A10Q1–Q4. The video amplifier output is applied to MEASUREMENT DEMOD VID OUT jack J14 for oscilloscope display, and also to the 50 percent pulse width detector which triggers interrogator decoder card A5, In the PRF CHAL position of the MEASUREMENT FUNCTION SEL switch the test set provides minimum amplification of input signals with sufficient power to provide a demodulated video output of at least l-volt amplitude at the MEASUREMENT DEMOD VID OUT jack. This level ensures maximum fidelity of the displayed signal. When MEASUREMENT FUNCTION SEL switch S31 is set to PWR, an adjustable bias from MEASUREMENT DEMOD VID LEVEL control R4 is applied. For power measurements, the MEASUREMENT DEMOD VID LEVEL control is adjusted until the power video signal at the MEASUREMENT DEMOD VID OUT jack is l-volt in amplitude, and is read out directly on MEASUREMENT meter Ml as peak power.

b. Frequency Measurement. Rf inputs to the SUM and DIFF RF IN/OUT and LOW POWER IN jacks, are coupled through attenuator AT4 and circulator HY3 to multicoupler DC3 to rf bit mixer A15. The 1090 MHz sweeping rf input signal (LO out) from the rf generator is also applied to rf bit mixer A15 and combined with the incoming signal. The rf bit mixer output is a 60-MHz signal which results when the local oscillator and the unknown frequency are exactly 60 MHz apart. Because in swept frequency operation the local oscillator is sweeping, a 60 MHz difference must exist at some point in the sweep. The 60 MHz signal is applied to 60 MHz if, amplifier AR1, and the amplified video is applied through filter FL1 to A10Q5 (fig. FO–15 sheet 2). When MEASUREMENT FUNCTION SEL switch S31 is set to FREQ, + 12v activates if detector A10Q5. The 60 MHz if signal is detected by A10Q5, amplified by video amplifiers A10Q1–Q4 and applied to the MEASUREMENT DEMOD VID OUT jack for display. The position of the displayed video signal in relation to the swept frequency markers, determines the frequency of the measured signal. During swept frequency operation and with MEASUREMENT FUNCTION SEL switch set to FREQ, pressing BIT (MOM) switch S37 activates rf bit A15. The 1030 MHz rf generator is activated and is combined with the swept local oscillator rf input signal from the rf signal generator. The resultant 60 MHz if signal is processed as previously described. The BIT (MOM) switch thus provides a check of the 60 MHz if filter amplifier and measurement circuitry, swept frequency markers and also rf bit Al 5.

c. *Interrogation Decoding* (fig. *2*– 14). To decode a challenge interrogation, the detected and amplified video is applied to the 50 percent pulse width detector, and the detector output drives the decoder logic. If the interrogation signal pulse spacing meets the criteria of the mode selected for decoding, a reply trigger is generated, The output of video amplifier A10Q1–Q4 is applied to the 50 percent pulse width detector consisting of delay line A10DL1, emitter-followers A10Q12, A10Q13, and A10Q14, and differential cornparator A10U5. The 50 percent pulse width detector timing is shown in figure 2– 14.

(1) The output of emitter-follower A10Q14 is applied to resistor network A10R53/R54/R56, and a threshold level of one-half the amplitude of the video

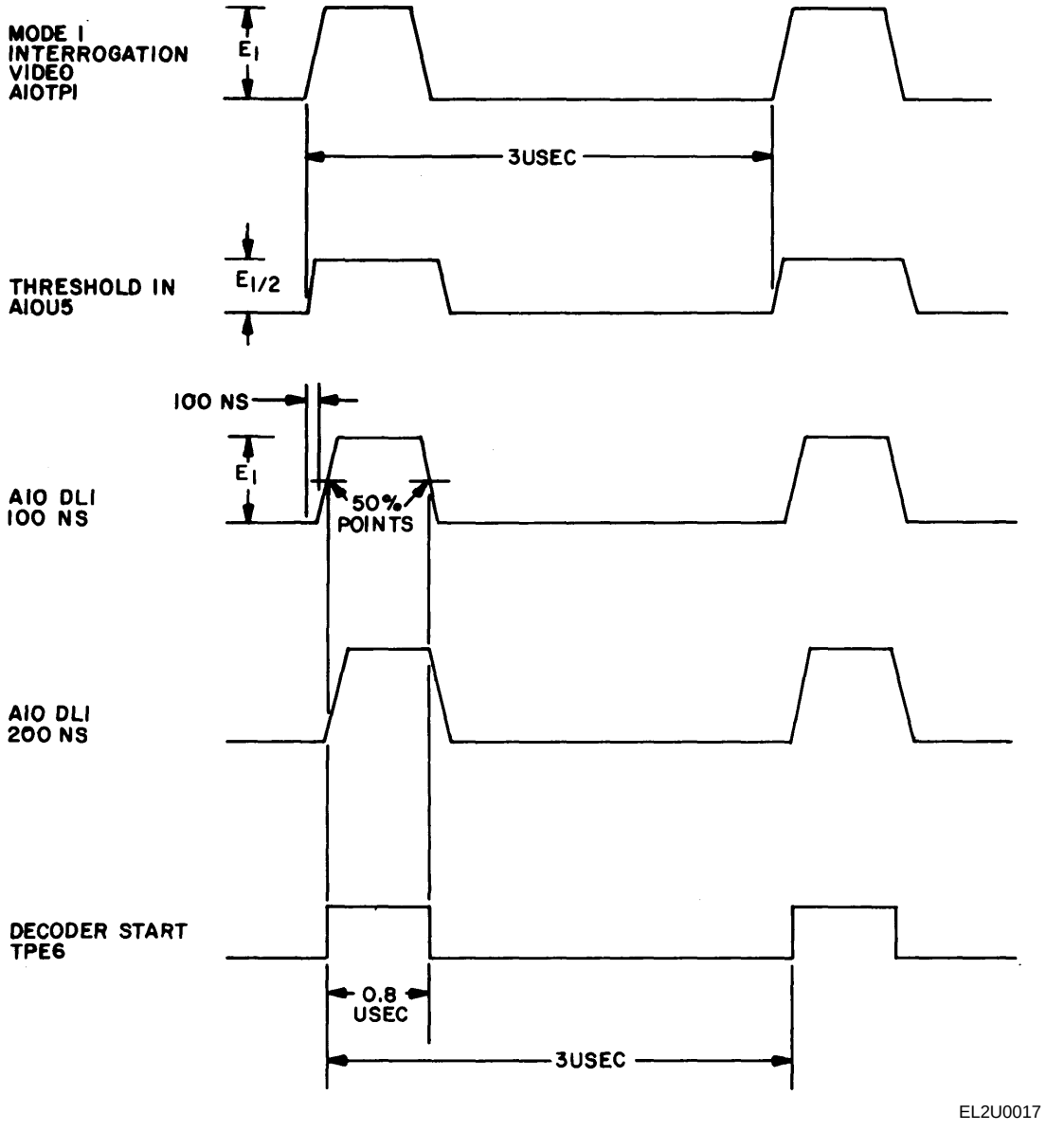

Figure 2-14. Pulse width discriminator timing diagram for model 1 interrogations.

pulse is established for differential comparator A10U5. The delay line is tapped at 100 and 200 nsec. The 100 nsec output is applied through emitter-follower A10Q12 to the comparator. When the leading edge of this input reaches the threshold level, the comparator output drops. At 200 nsec, the delay line output is applied through emitter-follower A10Q13 to the resistor network, maintaining the established threshold level. When the trailing edge of the 100 nsec input reaches threshold, the comparator output goes high. The output pulse of decoder start output amplifier A10Q15 represents the 50 percent points of the interrogation video pulse. The 50 percent video signal triggers shift register enable one-shot A5U3B through A5U1B. One-shot A5U3B clears decode shift register A5U7/U8/U9 and enables decode clock generator A5U4/U5. The clock 12 signal (10 MHz) input to decode clock generator A5U4/U5 is divided down to a 1 MHz clock and applied to the decode shift register and decode limit counter A5U16/U17/U18. The first 50 percent video pulse represents P1 of the interrogation signal and is clocked into the decode shift register.

Table 2-2 SIF Interrogation Pulse Pair Spacing.

Mode 1	3 usec
Mode 2	5 usec
Mode 3/A	8 usec
Mode C	21 usec

(2) In mode 4, the first 4 synchronizing pulses of the interrogation are spaced 2 use apart, and these are decoded. Assuming mode 1 interrogations are to be decoded, TRIG SEL DCD MODE SEL switch S27 is set to 1, and REPLIES MODULATION SEL switch S20 is set to SIF. The switch settings enable mode 1 decoding gate A5U12B through A5U10B. Each bit location of the decode shift register is 1 usec apart, only the locations pertinent to the decode operation are shown in figure FO–15. At each clock pulse, the PI pulse is shifted into the next bit location, If interrogation P3 pulse input to the test set generates a 50 percent video pulse 3 usec after P1, it is clocked into the decode shift register and the 0 and 3 usec outputs go high simultaneously and set counter latch A5U13B/U13C. Decode delay counter A5U16/U17/U18 is now enabled for the duration of the decode operation. On the next clock, the counter is incremented one count and output A goes high. When output A is low, the output of gate A5U2C is also low, When output A goes high, the output of gate A5U2C also goes high, triggering decode trigger shaper one-shot A5U3A. The one-shot generates two outputs; decoder trigger, which is applied to the Delay Generator Section initiating a reply, and decode reset, which resets counter latch A5U13B/U13C and the decode delay counter.

(3) Setting TRIG SEL DCD MODE SEL switch S27 to 2, 3/A, or C, enables the decoding gate for that mode. If the interrogation pulse spacing is correct, a decode trigger is generated (as described for mode 1), initiating a reply. Setting REPLIES MODULATION SEL switch S20 to I/P Ml and TRIG SEL DCD MODE SEL switch S27 to 1, enables mode 1 decoding and inhibits all other selected modes. Decoding a mode 1 interrogation generates a mode 1 I/P reply. Setting REPLIES MODULATION SEL switch S20 to I/P M2/3, enables mode 2 and 3/A decoding if TRIG SEL DCD MODE SEL switch S27 is set to 2, and inhibits all other selected modes, Decoding a mode 2 or 3/A interrogation generates a mode 2 or 3/A I/P reply. Setting REPLIES MODULATION SEL switch S20 to EMERG enables all SIF modes selected by TRIG SEL DCD MODE SEL switch S27, except mode C. Decoding a mode 1,2, or 3/A interrogation, generates an emergency reply.

(4) Setting TRIG SEL DCD MODE SEL switch S27 to 4 and REPLIES MODULATION SEL switch S20 to either M4–1P or M4–3P, enables mode 4 decoding gate A5U14 and raises the output of gate A5U2C. If the mode 4 interrogation synchronizing pulses are spaced 2 usec apart, counter latch A5U13B/U13C is set and the decode limit counter is enabled. The counter is incremented one count with each clock, but because output A does not affect the state of gate A5U2C, decode trigger shaper one-shot A5U3A is not triggered. The counter continues to increment for 192 µsec, at which time carry out goes high and then low, triggering one-shot A5U3A. A mode 4 reply is initiated and the counter latch and decode limit counter are reset. The mode 4 reply is a single pulse if REPLIES MODULATION SEL switch S20 is set to M4–lP, and a 3-pulse reply if set to M4-3P.

(5) Pressing BIT (MOM) switch S37 allows the operator to self-test the decoder. When BIT (MOM) switch S37 is pressed, the ST (self test) signal goes high and gates A5U2A/U2D are enabled. An sif chal trig signal is generated by a test set SIF interrogation mode with the SIF CHAL VID SIF MODE SEL switch as previously described, The decoder also functions as previously described, but instead of decoding a 50 percent video signal, the sif chal trig signal is directly decoded. The operator can determine proper decoding by the presence of a reply signal at REPLY VID OUT jack J6, when the TRIG SEL DCD MODE SEL switch is set to the mode corresponding to the interrogation mode. If the decoder is to be checked in mode 4, a mode 4 video signal is directly decoded in place of a 50 percent video signal. To prevent mode 4 challenge video presence simultaneously with SIF challenge video, the BIT (MOM) switch S37 disables mode 4 challenge video pulse width one-shot A3U6A unless the REPLIES MODULATION SEL switch is set to either M4–lP or M4–3P (fig. FO–4).

2 – 20. Measurement Section

(fig. FO-16)

The inputs to the measurement section from the Receiver Section, PRT Generator Section, or MEASUREMENT EXT VIDEO IN jack J9, are converted to prf or power indications which are displayed on MEASUREMENT meter Ml. When MEASUREMENT FUNCTION SEL switch S31 is set to PRF REPLY TRIG, gate A9U6A is enabled. The $\overline{0}$ trigger from the prt generator is applied through gates A9U6A and A9U8A to 100 µsec blanking one-shot A10U1. The 100 µsec duration of one-shot A10U1 allows only the first pulse of each pulse group to be counted. Therefore, each pulse group to be measured is converted into a single one-shot pulse which is independent of the number or width of the pulses being measured. The prf in signal triggers one-shot A10U1, which in turn triggers prf pulse shaper one-shot A10U2. The pulse from one-shot A10U2 is integrated by amplifier A10U3 into a dc level which is applied through amplifier A10Q8/Q9 to MEASUREMENT meter Ml. MEASUREMENT PRF RANGE switch S32 selects the range multiplier time constant for the prf range to be measured. The dc level applied to the meter is proportional to the ranged prf of the reply signal. When MEASUREMENT FUNCTION SEL switch S31 is set to PRF CHAL, 50 percent video triggers from the Receiver Section are transmitted by

transformer T1 is rectified by bridge rectifier PS1A1CR2/CR3 and provides a lamp supply voltage for DS3 DC FAULT indicator. Each power supply output is monitored by an over/under voltage sensor. The sensor inputs are provided to PS1A1U2/U3 which operate lamp driver PS1A1Q1/Q2. If an over/under voltage condition is sensed for any dc output, lamp driver A1Q1/Q2 lights DC FAULT indicator DS3.

b. +28V *output*. The secondary voltage of transformer T1 is rectified by PS1CR1/CR2, and applied to series regulator PS1A2Q1. Voltage reference amplifier PS1A1U1 controls current flow through the series regulator, maintaining the +28v output at a constant level. Over/under voltage sensor PS1A1U3 monitors the +28v output, and if an over/under voltage condition occurs, the sensor output drives the output of lamp driver PS1A1Q1/Q2 low, and the DC FAULT indicator lights.

c. *+12V output*. The secondary voltage of transformer T1 is rectified by bridge PSlCR3/CR6, and applied to series-regulator PS1A2Q2. Voltage reference amplifier PS1A1U4 controls current flow through the series regulator, maintaining the + 12v output at a constant level. Over/under voltage sensor PS1A1U2 monitors the +12v output, and if an over/under voltage condition occurs, the sensor output drives the output of lamp driver PS1A1Q1/Q2 low, and the DC FAULT indicator lights.

d. -12V output. The secondary voltage of transformer T1 is rectified by bridge PSlCR3/CR6, and applied to series-regulator PS1A2Q3. Voltage reference amplifier PS1A1U5 controls current flow through the series regulator, maintaining the - 12v output at a constant level. Over/under voltage sensor PS1A1U2 monitors the -12v output, and if an over/under voltage condition occurs, the sensor output drives the output of lamp driver PS1A1Q1/Q2 low, and the DC FAULT indicator lights.

e. *+5V output*. The secondary voltage of transformer T1 is rectified by PSlCR7/CR8, and applied to series regulator PS1Q1 and PS1Q2. Voltage sense amplifier PS1A1U6 controls current flow through the series regulator, maintaining the +5v output at a constant level. Over/under voltage sensor PS1A1U2 monitors the +5v output, and if an over/under voltage condition occurs, the sensor output drives the output of lamp driver PS1A1Q1/Q2 low, and the DC FAULT indicator lights.

A9U6C and A9U8A to 100 µsec blanking one-shot A10U1. A10U1 triggers A10U2 and applied a pulse to integrating amplifier A10U3, Q8, Q9 and MEASUREMENT meter Ml as described previously for a prf reply trig measurement. When MEASUREMENT FUNCTION SEL switch S31 is set to PRF EXT, gate A9U6D is enabled. Signals applied to MEASUREMENT EXT VID IN jack J9 are limited in amplitude by network TB2 and applied to driver A9Q1/Q2. The output of driver A9Q1/Q2 is gated through A9U6D, triggering one-shot A10U1, which triggers one-shot A10U2, applying a pulse to integrating amplifier A10U3, Q8, Q9 and MEASUREMENT meter Ml as described previously for a prf reply trig measurement. When MEASUREMENT FUNCTION SEL switch S31 is set to PWR, an adjusted video signal from MEASUREMENT DEMOD VID LEVEL control R4 is provided to M1A1 meter adjustment board where it is amplified, integrated and applied to MEASUREMENT meter Ml. For power measurements, the MEASUREMENT DEMOD VID LEVEL control R4 is adjusted until the video signal at the MEASUREMENT DEMOD VID OUT jack of the receiver is l-volt in amplitude when terminated by 75 ohms.

2–21. Power Supply

(fig, FO-17)

The power supply converts 115v, 45 to 70/380 to 420 Hz primary power into regulated dc outputs of +28, +12, -12 and +5 volts, The ac input power is fuse-protected against overload, and a power dc fault sensor circuit detects and gives an indication of an over/under voltage condition of any dc supply. The 115 vac primary power is applied through POWER connector Jl, EMI filter FL1/FL2, POWER ON/OFF switch S21, and POWER 1.5 AMP fuse F1 to power supply PS1. When power is applied, POWER indicator DS2 lights. If fuse F1 opens, the fuseholder neon lamp lights. If a dc supply over/under voltage condition exists, DC FAULT indicator DS3 lights. The primary power input to power supply PS1 is applied through EMI filter L1/L4 to the primary of transformer T1. Transformer T1 provides a secondary output for the power dc fault sensor, and the +28, +12, -12 and +5 volt outputs. The -12 volt output is derived from the same secondary as the +12v.

a. Power *Dc Fault Sensor.* The secondary output of

CHAPTER 3

GENERAL SUPPORT MAINTENANCE

Section I. GENERAL

3-1. Level of Maintenance

This chapter provides general support maintenance procedures for the test set. Included in this chapter are sections covering troubleshooting, removal and replacement, adjustment and alignment, repair, and general support testing.

3-2. Maintenance Forms and Records

Maintenance forms, records, and reports which are to be used by maintenance personnel at all maintenance levels are listed in and prescribed by TM 38–750.

3-3. Tools and Test Equipment

Tools and test equipment required for general support maintenance, repair parts, special tools, special test equipment, and accessories issued with or prescribed for use by the general support personnel for the AN/TPM–25A are listed in the maintenance allocation chart, in the appendixes of TM 11–6625–2610–12.

3-4. Equipment Preparation for Maintenance

The test set and equipment should be prepared for maintenance in the following procedures.

a. Test Set Connections, When performing performance test procedure (table 3 – 3) connect oscilloscope to test set as follows:

Oscilloscope jack	*Test Set jack*
A INPUT (with 134646–175–ohm termination)	RDR TRIG OUT
B INPUT (with 134646– 175–ohm termination)	REPLY VID OUT
MAIN EXT INPUT	MEASUREMENT SCOPE TRIG OUT

b. Test Set Control Settings. To prepare the test set for test, connect the power cable to 115 vac power source. Set the POWER ON/OFF switch to the ON position, Position the remaining controls as indicated in table 3-1.

Table 3–1. Test Set Control Settings

Controls	Settings
MEASUREMENT	
PRF RANGE	XIK
FUNCTION SEL	PRF REPLY TRIG
DEMOD VID LEVEL	Midrange
FREQ MEAS	Fully CW
EXT VID IN 75 Ω/2K Ω	*75 W*
REPLIES	
MODULATION SEL	SIF
REPLY WIDTH SELECT	0.45
REPLY WIDTH VARY	Midrange
SIF REPLY CODE	7700
SUB PULSE SEL	OFF
SUB PULSE POS SELECT	o
SUB PULSE POS VARY	Midrange
RANGE DELAY SEL (μSEC)	0001
GATING PASS	00
GATING INHIB	00
M4 JAMMING	0
PRT SELECT (μSEC)	
SIF CHAL VID SIF MODE SEL	OFF
SIF CHAL VID 5V/20V	5V
TRIG SEL INT/DCD/EXT	INT
TRIG SEL DCD MODE SEL	OFF
SIG GEN FUNCTION	FIXED FREQ
SIG GEN NORM/INTERLEAVE	NORM
SUM ATTEN	ODB
DIFF/INTERLEAVE ATTEN	ODB

c. Oscilloscope AN/USM–281A, Preparation for Use. To prepare the oscilloscope for use, connect the power cable to 115 vac, 50 to 100 Hz power source. Set POWER switch to the on position. Set remaining controls as indicated in table 3–2.

Table 3–2. Oscilloscope Control Settings

Controls	Settings
FIND BEAM	Released
INTENSITY	As required
FOCUS	As required
SCALE	As required
HORIZONTAL POSITION	As required
HORIZONTAL MAGNIFIER	Xl
HORIZONTAL DISPLAY	INT

Table 3–2. *Oscilloscope Control* Settings–Continued

Controls	Settings
HORIZONTAL AC/DC	DC
A POSITION	As required
A and B POLARITY	+ UP
DISPLAY	A
A AND B VOLTS/DIV	1
A AND B VOLTS/DIV vernier	CAL
MAGNIFIER	Xl
A AC/GND/DC	DC
MAIN VERNIER	CAL
RESET	Released
MAIN TRIGGER LEVEL	0
EXT + 10/EXT/INT/LINE	EXT
MAIN – SLOPE+	+
MAIN ACS/AFC/AC/DC	DC
MAIN TIME/DIV	.2 MSEC
DELAYED TIME/DIV	OFF
Sweep Display Switch	MAIN
SWEEP MODE	AUTO
DIV DELAY	0
DELAYED VERNIER	CAL
DELAYED TRIGGER LEVEL	0
DELAYED INT/AUTO/EXT/EXT ÷ 10	AUTO
DELAYED – SLOPE+	+
DELAYED ACS/ACF/AC/DC	DC

d. Dfferential Voltmeter ME–202B/U, Preparation for Use, To prepare the differential voltmeter for use, connect the power plug to a 115 vac power source. Set the NULL switch to VTVM and the OFF/ON/CAL switch to ON. Perform the preliminary operation procedure outlined in TM 11–6625–537–15.

e. *Frequency Counter AN/USM–207A, Preparation for Use.* To prepare the frequency counter for use, connect connector to a 115 vac power source. Set POWER switch to STBY and SENSITIVITY switch to lV. After a 10-minute warm-up period, set POWER switch to TRACK.

f. Frequency Comparator CM-77A/USM, Preparation for Use. To prepare the frequency comparator for use, connect the power plug to a 115 vac power source and set the POWER switch to ON. Connect OSCILLATOR OUTPUT to LOW FREQUENCY MIXER OSCILLATOR INPUT. Set the frequency comparator controls as directed *g* below.

g. Frequency Comparator CM-77A/USM, Control Settings. Set HORIZ SWEEP INPUT switch on rear panel to INT. Set the VIDEO RESPONSE GAIN and HIGH FREQUENCY controls fully c w. Adjust the HORIZ GAIN control for a full horizontal sweep on the display.

h. Pulse Generator AN/UPM–15A, Preparation for Use. To prepare the pulse generator for use, connect power connector to a 115 vac power source. Set POWER switch to ON. Set POLARITY switch to POS. Allow a 10-minute warmup period.

i. RF Power Meter AN/USM-260, Preparation for Use. To prepare the rf power meter for use, connect power connector to a 115 vac power source. Set LINE switch to ON. Allow a l5-minute warm-up period. Operate the rf power meter in accordance with the procedures contained in TM 11-6625-1549-12.

j. Signal Generator AN/URM–213, Preparation for Use. To prepare the signal generator for use connect the power connector to a 115 vac power source. Set POWER switch to ON. Allow a 10-minute warm-up period.

k. Pulse Power Calibrator Set AN/UPM-73, Preparation for Use.

CAUTION

BRIDGE and STANDARD SENSITIVITY switches should be set to OFF when not being used for BRIDGE measurements.

NOTE

Before applying power to pulse power calibrator set, ensure standard cell selector switch S8 (inside cabinet) is set to 1, 2, or *3*.

To prepare the pulse power calibrator set for use, con. nect the power cable connector to a 115 vac, 60 Hz power source. Set BRIDGE SENSITIVITY and STANDARD switches to OFF. Set STANDBY/OPERATE switch to STANDBY. Allow a two-hour warmup.

l. Interrogator Set AN/TPX–50 and Power Supply PP–2958A/U, Preparation for Use. To prepare the interrogator set and power supply for use, use the following procedure.

CAUTION

If interrogator generates rf with RF SUM or RF DIFF output disconnected (unloaded), damage to interrogator can result.

(1) Set power supply AC and DC switches to OFF. Adjust power supply output for 28 vdc.

NOTE

Maintain power supply output at 24 vdc minimum while operating interrogator set.

(2) Connect test setup as shown in figure 3–39.

(3) Set test controls per table 3-1 except set PRT SEL (µSEC) to 2500.

(4) Set receiver-transmitter RF PWR switch to HI.

(5) Set all interrogator group circuit breakers to ON.

(6) Set control box controls as follows:

Control	*Position*
CODE SELECT	
MODE 1	73
MODE 2	7777
MODE 3/A	7777
GTC ON	OFF
PANEL	OFF
POWER	ON
PROCESSOR	IN
MODE SELECT	3/A
SIF REPLIES	CODED
MODE 4	A

(7) Observe all interrogator set POWER indicators are on and after two minutes all SELF–TEST indicators are out.

Section II. TROUBLESHOOTING

3-5. General Troubleshooting Instructions

a. Troubleshooting at the general support maintenance level of the test set includes all the techniques outlined for organizational maintenance, and any special or additional techniques required to isolate a defective part. Systematic troubleshooting begins by performing the performance test procedure in table 3–3. When an abnormal indication is noted during performance of table 3-3, a reference is made to a corresponding malfunction in table 3–4 to sectionalize the trouble to a particular functional unit unless the functional unit is replaced and later repaired at a higher level maintenance facility. Important measuring points in the test set are brought out to convenient test points on the left side panel as shown in figure 3–1. Waveforms are provided in figure FO–22. Parts location information is provided in figures 3–2 through 3–5. Color codes for resistors, inductors, and capacitors is provided in figure FO–1. Wiring diagram information and cable diagrams are provided in figure FO–20.

b. To trace interconnections between schematic diagrams requires matching signal notations. With few exceptions, all inputs appear on the left and all outputs appear on the right side of the diagram. For example, on figure FO–3, sheet 1, to get to the destination of the M4 CLOCK signal line, the destination reference is given as SH 2, which implies figure FO–3, sheet 2, On sheet 2, signal line M4 CLOCK is located on the left (input) side and the source reference is given as SH 1, which implies figure FO–3, sheet 1, Another example is signal line SIF PRE TRIG which has a destination reference as figure FO–4. On figure FO–4 signal line SIF PRE TRIG is located on the left (input) side and the source reference is given as FO–3 (SH 1). One of the few exceptions of inputs (left side) and outputs (right side) on the schematic diagrams is shown on figure FO–3, sheet 1, upper left corner. In some cases the layout does not permit a convenient extension of the output signal lines to the right side of the diagram.

3-6. Organization of Troubleshooting

a. General. The first step in troubleshooting the test set is to sectionalize the fault (tracing the fault to a major functional unit). The second step is to localize the fault (tracing the fault to a defective part within the unit). Some faults, such as burned-out resistors, arcing, and shorted transformers can often be located by sight, smell, and hearing. The majority of faults, however, must be isolated by performing the performance test procedure in table 3–3

b. Sectionalization. For ease of troubleshooting, the equipment may be thought of as consisting of functional entities, each related electrically but categorized separately by the function performed, The first step in troubleshooting is to locate the function, or functions, at fault by the following methods:

(1) *Visual inspection,* The purpose of the visual inspection is to locate faults without testing or measuring the circuits. All visual signs should be observed and an attempt made to sectionalize the fault to a particular function.

(2) *Fault localization test.* The performance test procedure (table 3–3) frequently indicates the general location of the trouble. In many instances, the test will help in determining the exact nature of the fault.

c. *Localization.* The tests listed in the following paragraphs will aid in localizing the trouble. First, localize the trouble to a single function, and then isolate the trouble within that circuit by waveform, voltage, resistance, and continuity measurements.

(1) *Troubleshooting chart.* When used with the performance test procedure, continuity measurements, and the waveform diagram (fig. FO–22), the troubleshooting information in table 3-4 will aid the technician in localizing troubles to a component part. Defective components identified by performing correction action are replaced with a known reliable component unless repair or other disposition is noted. The corrective action column references data tables, if required, for checking components; otherwise, refer to schematics and wiring diagrams when performing checks. Once the action indicated in the corrective action has been accomplished, the performance test procedure where the fault was first noted should be re-performed to insure that the fault has been corrected.

(2) *Waveform measurements* (fig. FO–22). An

A	FROM
1 COUNTER	A1-13
2 ZERO TRIG	A1-11
3 MAX PRF REPLY GATE	A1-9
4 SIF PRE TRIG	A1-33
5 SIF GATE	A1-20
6 M4 GATE	A1-21
7 SIF CLOCK	A1-6
8 M4 CLOCK	A1-8
9 M4 INT REF	A2-6
10 M4 CHAL	A2-33

B	FROM
1 REPLY TRIG	A2-4
2 ENABLE TRIG	A2-11
3 SIF CHAL TRIGS	A2-23
4 BLANKING RESET	
5 SWEEP START	A3-25
6 SWEEP CLOCK SYNC	A3-43
7	
8 RANGE COUNTER COMPOSITE	A4-26
10 M4 ENABLE	A5-16

C	FROM
1 DECODE TRIG	A5-32
2 SIF SELECT	A5-34
3 SIF ENABLE	A5-43
4 M4 SELECT	A5-50
5 GATED JAMMING TRIG	A6-38
6 M4 FT (FIXED TARGET)	A6-41
7 E SUB	A6-46
8 SLIDING TRIG	A7-4
9 M4 SHIFT CLOCK	A7-7
10 M4 REPLY& SUB TRIG	A7-8

D	FROM
1 JAMMING TRIG	A7-11
2 SIF ZERO CLOCK	A7-14
3 REPLY TRIGS	A8-4
4 EARLY SUB GATE	A8-45
5 AUX MOD	A9-19
6 MAIN MOD	A9-20
7 E TRIG	A9-22
8 PRF (METER)	A9-23
9	
10 AMPLIFIER/FILTER (+ 12 VDC)	TB3-E17

E	FROM
1	
2	
3	
4 DETECTOR INPUT	A10-39
5 DETECT IF INPUT	A10-24
6 50% VIDEO WIDTH	A10-5
7 IF INPUT	A10-32
8	
10	

F	FROM
1 MODULATOR, +SUM/MAIN	A16A1-E16
2 MODULATOR, -SUM/MAIN	A16A1-E18
3 MODULATOR, +DIFF/AUX	A16A1-E11
4 MODULATOR -DIFF/AUX	A16A1-E13
5 DETECTOR AMPLIFIER INPUT	AR2-P6-7
6 RAMP OUT	A11A1-P5-13
7 POSITIVE GATE OUT	A11A1-P5-8
8 GROUND	
9 RF BIT (+12 VDC)	TB3-E5
10 RF BIT(+12 VDC)	A15-FL2

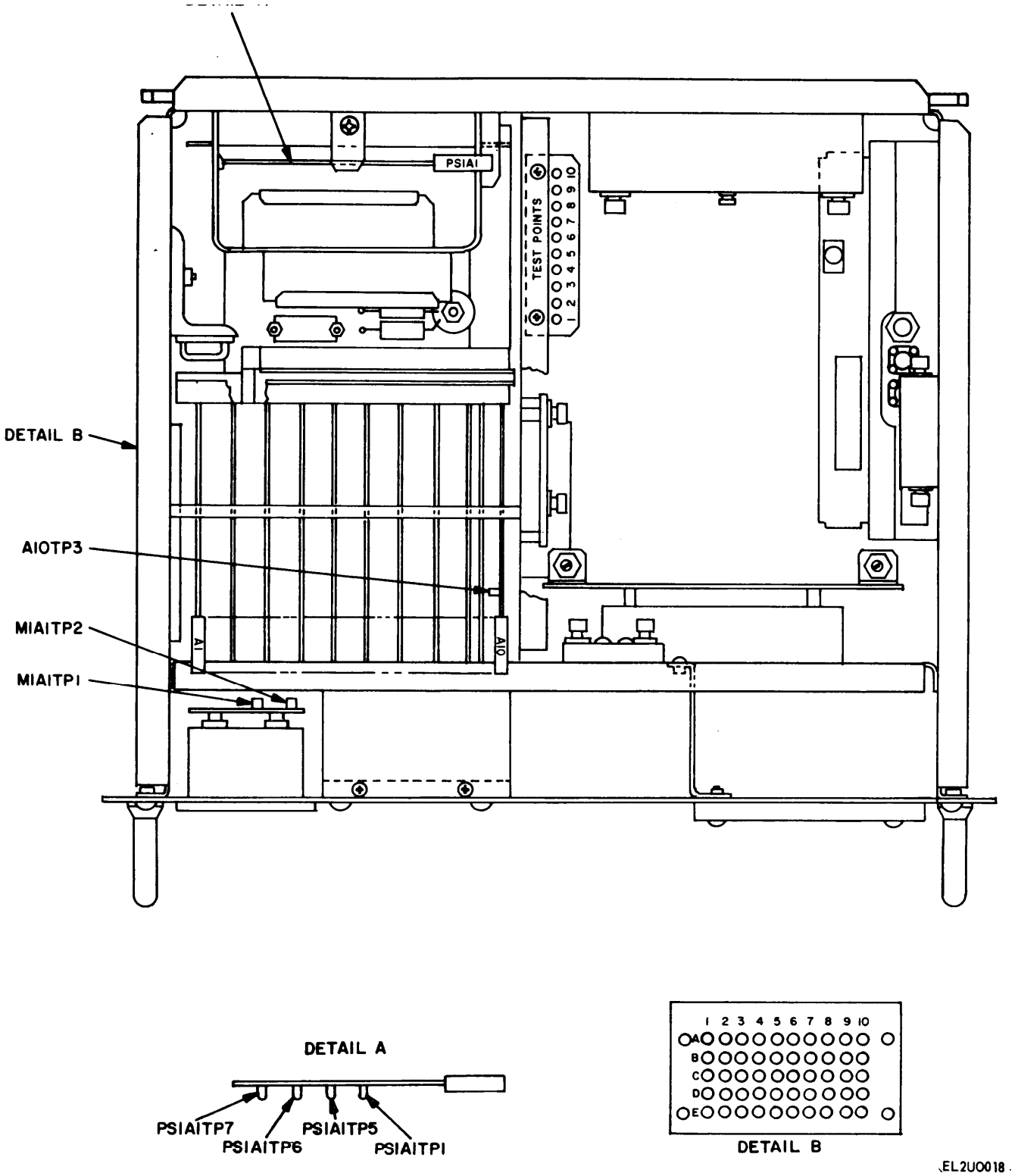

Figure 3-1. Test point location diagram.

oscilloscope is used for observing waveforms at appropriate test points. The waveforms on figure FO-22 illustrate the waveforms obtained at the test points of the test set.

(3) *Voltage and resistance measurements.* A multimeter is used for taking voltage and resistance measurements on the chassis.

CAUTION

When making voltage measurements of transistors, use tape or sleeving to insulate the test probe except for the extreme tip, to prevent accidental shorting of the test probe to the chassis (even a momentary short circuit can damage the transistor).

(4) *Continuity checks.* Routine continuity checks between various points in the circuitry can be made using multimeter and the wiring diagrams.

(5) *Intermittent troubles.* When troubleshooting, the possibility of intermittent troubles should not be overlooked. This trouble can often be made to appear by tapping or jarring the equipment. Check wiring and connections,

3-7. Interunit Troubleshooting

a. Defective Signal Monitoring. Failure to monitor a selected voltage or signal may be caused by defective external test equipment. If an operational check fails to sectionalize trouble to a defective major functional area, follow the procedures given in (b), (c) and *(d)* below.

b. External test equipment check. All external test equipment should function properly. Perform operational checks on each unit of external test equipment as described in the applicable test equipment manual.

c. Controls. To verify that all controls are functioning properly, perform continuity measurements while the controls are rotated through each position.

d. Checking cable assemblies. All interconnecting cable assemblies should be checked for signs of insulation deterioration and for opens or shorts near the connectors. Check connectors for bent or deformed pins and for signs of arcing.

Table 3–3. Performance Test Procedure

step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3– 4
1	Set up oscilloscope as described in paragraph 3–4c..	Set up test set as described in paragraph 3–4a and *b.*	Power Supply Test *a.* Observe POWER 1.5 AMPS fuseholder.	*a.* POWER 1.5 AMPS fuseholder is extinguished.	Malfunction 1
			b. Observe POWER indicator.	*b.* POWER indicator is lit.	Malfunction 2
			c. Observe POWER DC FAULT indicator.	c. POWER DC FAULT indicator is extinguished.	Malfunction 3
			d. Press DC FAULT indicator.	*d.* DC FAULT indicator lights when pressed.	Malfunction 8
2			PRT and PRF Measurement Test *a.* Observe MEASUREMENT meter indication.	*a.* MEASUREMENT meter indicates 1.9 to 2.1 on the Hz scale.	Malfunction 9
		PRT SEL (µSEC) switches: 1100. MEASUREMENT PRF RANGE switch: X100.	*b.* Set PRT SEL (µSEC) switches to following positions and observe MEASUREMENT meter indication. (1) 1100 (2) 1200 (3) 1400 (4) 1800 (5) 2000 (6) 4000 (7) 8000	*b.* MEASUREMENT meter indicates as follows on Hz scale: (1) 8.6 to 9.6 (2) 7.8 to 8.8 (3) 6.6 to 7.6 (4) 5.0 to 6.1 (5) 4.5 to 5.5 (6) 2.25 to 2.75 (7) 1.1 to 1.4	Malfunction 9
		PRT SEL (µSEC) switches: 9999. MEASUREMENT PRF RANGE switch: X10.	c. Observe MEASUREMENT meter indication.	c. MEASUREMENT meter indicates 9.5 to full scale on Hz scale.	Malfunction 9

Table 3–8. Performance Test Procedure-Continued

step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3-4
3	DISPLAY switch: A. MAIN TIME/ DIV switch: .5 µSEC, DELAYED TIME/DIV switch: OFF. MAIN EXT ÷ 10/EXT/INT/ LINE switch: INT. Sweep delay switch: MAIN.		Scope Trigger *a.* Disconnect 75 Ω termination from oscilloscope A INPUT. *b.* Disconnect video cable from oscilloscope MAIN EXT jack and connect with 93 Ω termination to A INPUT. c. Adjust oscilloscope DIV DELAY control to observe pulse.	c. (1) Pulse present. (2) Pulse amplitude is 5.0 ± 1.0 volt. (3) Pulse width is 1.0 to 5.0 µsec.	Malfunction 12 Malfunction 14 Malfunction 14
4	DISPLAY switch: ALT. A VOLTS/ DIV switch: 5. MAIN EXT ÷ 10/EXT/INT/ LINE switch: EXT.	MEASUREMENT PRF RANGE switch: X100. PRT SEL (µSEC) switches: 4000.	Radar Trigger Output Test a. Remove video cable and 93 Ω termination from A INPUT *.a.* and connect cable to oscilloscope MAIN EXT jack. ***b.*** Reconnect 75 Ω termination and video cable from test set RDR TRIG OUT jack to oscilloscope A INPUT.		
	MAIN TIME/ DIV switch: 50 ASEC.		c. Observe pulse amplitude. Observe width at 50% amplitude of pulse. *d.* Note delay between pulse on A INPUT and first pulse on B INPUT.	c. A input amplitude is 10 v ± 1 v and width is 3 µsec ± 1 µsec. *d.* Nominal delay is 434 µsec ± 0.2 µsec. (Actual tolerance is beyond oscilloscope accuracy; for this test measure to ± 20 µsec). **NOTE** Adjustable from 360.0 µsec to 438.0 µsec. This is a nominal setting and may change with different interrogator systems.	Malfunction 15 Malfunction 16 or malfunction 24
5	MAIN TIME/ DIV switch: 2 MSEC.	REPLIES GATING PASS switch: 01. REPLIES GATING INHIB switches: 01. PRT SEL (µSEC) switches: 1000. MEASUREMENT FUNCTION SEL switch: PRF EXT.	Replies Gating Test *a.* Observe ratio of radar trigger pulses on A INPUT to reply pulse trains on B INPUT. *b.* Disconnect cable from oscilloscope B INPUT, remove termination, and connect to test set MEASUREMENT EXT VID IN jack. c. Observe test set.	*a.* One reply pulse train on B INPUT for every other radar trigger pulse on A INPUT. *b.* None. c. Meter indicates 500 Hz± 50 Hz.	Malfunction 26 Malfunction 27

Table 3–3. Performance Test Procedure-Continued

Step No.	Control settings		Test procedures	Performance standard	If indication is abnormal see table *3–4*
	Oscilloscope	Test set			
5 (cont.		REPLIES GATING PASS switches: 02. REPLIES GATING INHIB switches: 02.	*d.* Observe test set meter.	*d.* Meter indicates 500 Hz ± 50 Hz	Malfunction 26
		REPLIES GATING PASS switches: 03. REPLIES GATING INHIB switches: 03	*e.* Observe test set meter.	*e.* Meter indicates 500 Hz ± 50 Hz.	Malfunction 26
		REPLIES GATING PASS switches: *04.* REPLIES GATING INHIB switches: 04.	*f.* Observe test set meter.	*f.* Meter indicates *500* Hz ± *50* Hz.	Malfunction *26*
		REPLIES GATING PASS switches: 05. REPLIES GATING INHIB switches: 05.	*g.* Observe test set meter.	*g.* Meter indicates 500 Hz ± *50* Hz.	Malfunction 26
		REPLIES GATING PASS switches: 06. REPLIES GATING INHIB switches: 06.	*h.* Observe test set meter.	*h.* Meter indicates 500 Hz ± *50* Hz.	Malfunction *26*
		REPLIES GATING PASS switches: 07. REPLIES GATING INHIB switches 07.	*i.* observe test set meter.	*i.* Meter indicates 500 Hz ± 50 Hz.	Malfunction *26*
		REPLIES GATING PASS switches: 08. REPLIES GATING INHIB switches: 08.	j. Observe test set meter.	*j.* Meter indicates *500* Hz ± *50* Hz.	Malfunction *26*
		REPLIES GATING PASS switches: 09. REPLIES GATING INHIB switches: 09.	*k.* Observe test set meter,	*k.* Meter indicates 500 Hz ± *50* Hz.	Malfunction *26*
		REPLIES GATING PASS switches: 10. REPLIES GATING INHIB switches: 10.	*l.* Observe test set meter.	. Meter indicates 500 Hz ± *50* Hz.	Malfunction *26*
			m. Set REPLIES GATING PASS and INHIB switches to following positions and observe meter indications.	*m.* Meter indicates 500 Hz ± 100 Hz (meter will fluctuate).	Malfunction 26

Table 3–3 Performance Test Procedure-Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3–4
5 (cont.			*PASS* / *INHIBIT* 20 / 20 30 / 30 40 / 40 50 / 50 60 / 60 70 / 70 80 / 80 90 / 90		
6			Range Delay Test	NOTE For steps *b* thru *j* below,	
	MAIN TIME/ DIV switch: .2 MSEC.	REPLIES RANGE DELAY SEL (µSEC) switches: 1111.	*a.* Disconnect cable from test set MEASUREMENT EXT VID IN jack and connect with 75-ohm termination to oscilloscope B INPUT.	is the sum of the SIF sys nally set to 434 Met) and by the REPLIES RANGE switches (minus the nomi deviation from nominal is specific system parameters system under test. The SIB adjustable over a range of 3	the specified delay tem delay (nomi- the range selected DELAY SEL nal setting). The determined by the of the interrogator system delay is to 438 µsec.
		PRT SEL (µSEC) switches: 4000. REPLIES GATING PASS switches: 00. REPLIES GATING INHIB switches: 00.	*b.* Observe delay between pulse on A INPUT and first pulse on B INPUT,	*b.* Delay is 1544 µsec ± 0.6 µsec (actual tolerance is beyond oscilloscope accuracy, for this test measure to ± 50 µSEC).	Malfunction 28
	MAIN TIME/ DIV switch: .5 MSEC.	REPLIES RANGE DELAY SEL (µSEC) switches: 2222.	*c.* Observe delay between pulse on A INPUT and first pulse on B INPUT.	*c.* Delay is 2655 µsec ± 0.6 µsec (actual tolerance is beyond oscilloscope accuracy, for this test measure to ± 60 µsec).	Malfunction 28
	MAIN TIME/ DIV switch: .1 MSEC.	REPLIES RANGE DELAY SEL (µSEC) switches: 0333.	*d.* Observe delay between pulse on A INPUT and first pulse on B INPUT.	*d.* Delay is 766 µsec ± 0.2 µsec (actual tolerance is beyond oscilloscope accuracy, for this test measure to ± 25 µsec).	Malfunction 28
		REPLIES RANGE DELAY SEL (µSEC) switches: 0444.	*e.* Observe delay between pulse on A INPUT and first pulse on B INPUT.	e. Delay is 877 µsec ± 0.2 µsec (actual tolerance is beyond oscilloscope accuracy, for this test measure to ± 25 µsec).	Malfunction 28
		REPLIES RANGE DELAY SEL (µSEC) switches: 0555.	*f.* Observe delay between pulse on A INPUT and first pulse on B INPUT.	*f.* Delay is 988 µsec ± 0.2 µsec (actual tolerance is beyond oscilloscope accuracy, for this test measure to ± 25 µsec).	Malfunction 28

Table 3–3. Performance Test Procedure-Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3-4
6 (cont.)	MAIN TIME/ DIV switch: .2 MSEC.	REPLIES RANGE DELAY SEL (µSEC) switches:	g. Observe delay between pulse on A INPUT and first pulse on B INPUT.	*g.* Delay is 1099 µsec ± 0.2 µsec (actual tolerance is beyond oscilloscope accuracy, for this test measure to ± *50 µsec).*	Malfunction 28
		REPLIES RANGE DELAY SEL (µSEC) switches: 0777.	*h.* Observe delay between pulse on A INPUT and first pulse on B INPUT,	*h.* Delay is 1210 µsec ± 0.2 µsec (actual tolerance is beyond oscilloscope accuracy, for this test measure to ± 50 µsec).	Malfunction 28
		REPLIES RANGE DELAY SEL (µSEC) switches: 0838.	*i.* Observe delay between pulse on A INPUT and first pulse on B INPUT.	*i.* Delay is 1321 µsec ± 0.2 µsec (actual tolerance is beyond oscilloscope accuracy for this test measure to ± 50 µsec).	Malfunction 28
		REPLIES RANGE DELAY SEL (µSEC) switches: 0999.	*j.* Observe delay between pulse on A INPUT and first pulse on B INPUT.	*j.* Delay is 1432 µsec ± 0.2 µsec (actual tolerance is beyond oscilloscope accuracy for this test measure to ± 50 µsec).	Malfunction 28
7			SIF Reply Pulse Train		
	DISPLAY switch: B. A VOLTS/ DIV switch: 2. B VOLTS/ DIV switch: 1. MAIN TIME/ DIV switch: 50 µSEC. DELAYED TIME/DIV switch: 5 µSEC. Sweep display switch: DELAYED	REPLIES RANGE DELAY SEL (µSEC) switches: 0001. PRT SEL (µSEC) switches: 0500. REPLIES SIF REPLY CODE switches: 7777.	*a.* Adjust oscilloscope DIV DELAY control until reply pulse train is centered on oscilloscope screen.	*a.* Oscilloscope displays 14-pulse reply train. Amplitude is 5 v ± 0.5 v.	Malfunction 29 or malfunction 30
	DELAYED TIME/DIV switch:.1 µSEC.		*b.* Adjust oscilloscope DIV DELAY control until one pulse is centered on oscilloscope screen. Observe pulse width at 50% of pulse amplitude.	*b.* Pulse width is 0.45 µsec ± 0.05 µsec.	Malfunction 31
		REPLIES REPLY WIDTH switch: 0.15.	c. Observe pulse width at 50% of pulse amplitude.	*c.* Pulse width is 0.15 µsec ± 0.05 µsec.	Malfunction 31
		REPLIES REPLY WIDTH switch: 0.50	*d.* Observe pulse width at *50%* of pulse amplitude.	*d.* Pulse width is 0.50 µsec ± 0.05 µsec.	Malfunction 31

Table 3-3. Performance Test Procedure—Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3–4
7 (cont.)		REPLIES REPLY WIDTH switch: 0.90.	*e.* Observe pulse width at 5090 of pulse amplitude.	e. Pulse width is 0.90 µsec +0.05 µsec.	Malfunction 31
	DELAYED TIME/DIV switch: .2 µSEC.	REPLIES REPLY WIDTH switch: VARY.	*f.* Adjust REPLIES REPLY WIDTH VARY control while observing pulse width.	*f.* Pulse width varies from less than 0.15 µsec to more than 1.5 µsec.	Malfunction 31
	DELAYED TIME/DIV switch: 5 µSEC.	REPLIES REPLY WIDTH switch: 0.50.			
		REPLIES SIF REPLY CODE switches: 0000.	*g.* Adjust oscilloscope DIV DELAY control to observe two bracket pulses on B INPUT.	g. Pulse spacing is 20.30 µsec ± 0.02 µsec. Actual tolerance beyond oscilloscope accuracy, for this test measure to ± 1.0 µsec.	Malfunction 32
8			SIF Reply Substitute Pulse Test		
		REPLIES SIF REPLY CODE switches: 0010.	*a.* Adjust oscilloscope DIV DELAY control to observe two bracket pulses and a C1 pulse following the first bracket pulse on B INPUT.	*a.* Two bracket pulses and a C1 pulse following the first bracket pulse.	Malfunction 33
		REPLIES SUB PULSE SEL switch: C1.			
	DELAYED TIME/DIV switch: .2 µSEC.		b. Measure pulse spacing between first bracket pulse and C1 pulse.	a. Pulse spacing is 1.45 µsec ± 0.02 µsec.	Malfunction 33
		REPLIES SUB PULSE POS SELECT switch: -.50.	*c.* Adjust oscilloscope DIV DELAY control to measure pulse spacing between first bracket pulse and C1 pulse.	*c.* Pulse spacing is 0.95 µsec ± 0.02 µsec.	Malfunction 33
		REPLIES SUB PULSE POS SELECT switch: -.35.	*d.* Adjust oscilloscope DIV DELAY control to measure pulse spacing between first bracket pulse and C1 pulse.	*d.* Pulse spacing is 1.10 µsec ± 0.02 µsec.	Malfunction 33
		REPLIES SUB PULSE POS SELECT switch: -.25.	*e.* Adjust oscilloscope DIV DELAY control to measure pulse spacing between first bracket pulse and C1 pulse.	*e.* Pulse spacing is 1.20 µsec ± 0.02 µsec.	Malfunction 33

Table 3–3. Performance Test Procedure-Continued

Step No.	Control settings		Test procedures	Performance standard	If indication is abnormal see table 3–4
	Oscilloscope	Test set			
8 (cont.)		REPLIES SUB PULSE POS SELECT switch: -.15.	*f.* Adjust oscilloscope DIV DE LAY control to measure pulse spacing between firs bracket pulse and Cl pulse.	*f.* Pulse spacing is 1.30 µsec ± 0.02 µsec.	Malfunction 33
		REPLIEs SUB PULSE POS SELECT switch: +.15.	*g.* Adjust oscilloscope DIV DE-LAY control to measure pulse spacing between first bracket pulse and Cl pulse.	*g.* Pulse spacing is 1.60 µsec ± 0.02 µsec.	Malfunction 33
		REPLIES SUB PULSE POS SELECT switch: +.25.	*h.* Adjust oscilloscope DIV DE-LAY control to measure pulse spacing between first bracket pulse and Cl pulse.	*h.* Pulse spacing is 1.70 µsec ± 0.02 µsec.	Malfunction 33
		REPLIES SUB PULSE POS SELECT switch: + .35.	*i.* Adjust oscilloscope DIV DE LAY control to measure pulse spacing between firs bracket pulse and Cl pulse.	Pulse spacing is 1.80 µsec ± 0.02 µsec.	Malfunction 33
		REPLIES SUB PULSE POS SELECT switch: +.50.	*j.* Adjust oscilloscope DIV DE LAY control to measure pulse spacing between first bracket pulse and Cl pulse.	Pulse spacing is 1.95 µsec ± 0.02 µsec.	Malfunction 33
		REPLIES SUB PULSE POS SELECT switch: VARY.	*k.* Adjust REPLIES SUB PULSE POS VARY control while observing first bracket pulse and Cl pulse.	Spacing varies from less than 0.65 µsec to more than 2.25 µsec.	Malfunction 33
	DELAYED TIME/DIV switch: .1 µSEC.	REPLIES REPLY WIDTH SELECT switch: 0.15.	*l.* Adjust oscilloscope DIV DE-, LAY control until Cl pulse is centered on oscilloscope screen. Observe pulse width at 50% of pulse amplitude.	Pulse width is 0.15 µsec ± 0.05 µsec.	Malfunction 34
		REPLIES REPLY WIDTH SELECT switch: 0.45.	*m.* Observe pulse width at 50% of pulse amplitude.	Pulse width is 0.45 µsec ± 0.05 µsec.	Malfunction 34
		REPLIES REPLY WIDTH SELECT switch: 0.50.	*n.* Observe pulse width at 50% of pulse amplitude.	*n.* Pulse width is 0.50 µsec ± 0.05 µsec.	Malfunction 34

Table 3–3. *Performance Test* Procedure—Continued

Step No,	Control settings		Test procedures	Performance standard	If indication is abnormal see table 3–4
	Oscilloscope	Test set			
8 (cont.)		REPLIES REPLY WIDTH SELECT switch: 0.90.	o. Observe pulse width at 50!Z0 of pulse amplitude.	*o.* Pulse width is 0.90 µsec ± 0.05 µsec.	Malfunction 34
	DELAYED TIME/DIV switch:.2 µSEC.	REPLIES REPLY WIDTH SELECT switch: VARY.	p. Adjust REPLIES REPLY WIDTH VARY control while observing pulse width.	*p.* Pulse width varies from less than 0.15 µsec to more than 1.50 µsec.	Malfunction 34
	DELAYED TIME/DIV switch: 5 µSEC.	REPLIES SIF REPLY CODE switch: 7777. REPLIES REPLY WIDTH SELECT switch: 0.50. REPLIES SUB PULSE POS SELECT switch: +.50.	q. Adjust oscilloscope DIV DELAY control to center reply pulse train display. Set test set REPLIES SUB PULSE SEL switch to each position through BRKT–2 while observing each pulse of 14-pulse train.	*q.* Pulse corresponding to each REPLIES SUB PULSE SEL switch setting moves when selected.	Malfunction 36
9			Mode 4 Reply Test		
	DELAYED TIME/DIV switch: 1 µSEC.	REPLIES MODULATION SEL switch: M4–3P.	*a.* Adjust oscilloscope DIV DELAY control to observe 3-pulse train.	*a.* Oscilloscope displays 3-pulse train.	Malfunction 37 or Malfunction 63
	DELAYED TIME/DIV switch:.2 µSEC.	REPLIES SUB PULSE SEL switch: OFF.	*b.* Measure pulse spacing (Pl to P2 and P2 to P3).	*b.* Pulse spacing is 1.8 µsec +0.05 µsec.	Malfunction 42
	DELAYED TIME/DIV switch:.5 µSEC.	REPLIES SUB PULSE SEL switch: M4-P2.	*c.* Observe position of second (P2) pulse.	*c.* P2 pulse moved +0.50 psec ± 0.02 µsec.	Malfunction 43
		REPLIES SUB PULSE SEL switch: M4–P3.	*d.* Observe position of second (P2) and third (P3) pulses.	*d.* P2 pulse returns to original position and P3 pulse moves + 0.50 µsec ± 0.02 µsec.	Malfunction 43

Table 9–9. Performance Test Procedure—Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3– 4
9 (cont.)		REPLIES SUB PULSE SEL switch: OFF. REPLIES MODULATION SEL switch: M4-lP.	*e.* Observe only one pulse remains.	*e.* One pulse displayed.	Malfunction 44
10			Mode 4 Jamming Test		
	DELAYED TIME/DIV switch: 10 µPSEC.	REPLIES M4 JAMMING switch: 1.	*a.* Adjust oscilloscope DIV DELAY control to observe 3 jamming pulses appear with reply pulse.	*a.* Oscilloscope displays 3 jamming pulses followed by reply pulse. NOTE In steps *a* thru e the jamming pulses are counted down (baseline present) and the mode 4 one pulse reply is solid (no baseline).	Malfunction 45
		REPLIES M4 JAMMING switch: 2.	*b.* Observe 6 jamming pulses appear with reply pulse.	*b.* Oscilloscope displays 6 jamming pulses with reply pulse.	Malfunction 45
		REPLIES M4 JAMMING switch: 3.	*c.* Observe 9 jamming pulses appear with reply pulse.	*c.* Oscilloscope displays 9 jamming pulses with reply pulse.	Malfunction 45
		REPLIES M4 JAMMING switch: 4.	*d.* Observe 12 jamming pulses appear with reply pulse.	*d.* Oscilloscope displays 12 jamming pulses with reply pulse.	Malfunction 45
		REPLIES M4 JAMMING switch: 5.	*e.* Observe 15 jamming pulses appear with reply pulse.	*e.* Oscilloscope displays 15 jamming pulses with reply pulse,	Malfunction 45
11			Identification Position Test		
	DELAYED TIME/DIV switch: 5 µSEC.	REPLIES M4 JAMMING switch: 0. REPLIES MODULATION SEL switch: I/P Ml.	*a.* Adjust oscilloscope DIV DELAY control to view two complete pulse trains.	*f.* Two reply pulse trains are displayed; spacing between first pulse of each train is 24.65 µsec ± 0.05 µsec.	Malfunction 48
		REPLIES MODULATION SEL switch: I/P M2/3.	b. Observe reply train followed by single pulse on oscilloscope.	*g.* One reply train followed by single pulse is displayed; spacing between first pulse of reply train and single pulse is 24.65 µsec ± 0.05 µsec.	Malfunction 48

Table 3–3. Performance Test Procedure-Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3–4
12	MAIN/TIME/DIV switch: .1 MSEC. DELAYED TIME/DIV switch: 10 µSEC.	PRT SEL (µSEC) switches: 1500. REPLIES MODULATION SEL switch: EMERG.	Emergency Reply Test Adjust oscilloscope DIV DELAY control to view complete pulse train.	One reply train followed by three sets of bracket pulses.	Malfunction 48
13	DELAYED TIME/DIV switch: 5 µSEC.	REPLIES MODULATION SEL switch: GARBLE. REPLIES SUB PULSE SEL switch: BRKT–2.	Garble Reply Test Observe oscilloscope. Measure spacing between last pulse of reply train and single pulse. Adjust oscilloscope DIV DELAY control to observe entire pulse train.	One reply train followed by single pulse is displayed. Spacing between last pulse of reply train and single pulse is 20.30 µsec ±0.05 µsec.	Malfunction 49
14		REPLIES MODULATION SEL switch: 30 **KHz.** REPLIES SUB PULSE SEL switch: OFF. REPLIES SUB PULSE **POS** switch: 0.	Output Pulsing Test Observe oscilloscope,	Pulse occurs every 30 µsec to 37 µsec. NOTE A double pulse is observed within the 30 KHz display. Ignore this double pulse for this measurement.	Malfunction 50
15	DELAYED TIME/DIV switch: 1 µSEC.	SIF CHAL VID SIF MODE SEL switch: 1.	SIF Challenge Video Output Test *a.* Disconnect cable from test set REPLY VID OUT jack and connect to SIF CHAL VID CHAL VID OUT jack.	*a.* None.	
			b. Adjust oscilloscope DIV DELAY control to observe 2 challenge pulses on B INPUT and measure pulse spacing, amplitude and width.	*b.* (1) Two pulses present. (2) Pulse spacing is 3.0 µsec ±0.1 µec, (3) Pulse amplitude is +5.0 v ±0.5 v, (4) Pulse width is 0.80 µsec ±0.05 µsec.	Malfunction 52 Malfunction 56 Malfunction 54 Malfunction 55

Table 3–3. Performance Test Procedure-Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3–4
15 (cont.)		SIF CHAL VID SIF MODE SEL switch: 2.	c. Observe oscilloscope. Measure pulse spacing.	c. Pulse spacing is 5.0 µsec ± 0.1 µsec.	Malfunction 56
		SIF CHAL VID SIF MODE SEL switch: 3/A.	*d.* Observe oscilloscope. Measure pulse spacing.	*d.* Pulse spacing is 8.0 µsec ± 0.1 µsec.	Malfunction 56
	DELAYED TIME/DIV switch: 5 µSEC.	SIF CHAL VID SIF MODE SEL switch: C.	*e.* Observe oscilloscope. Measure pulse spacing.	*e.* Pulse spacing is 21.0 µsec ± 0.1 µsec.	Malfunction 56
	B INPUT VOLTS/DIV switch: 5.	SIF CHAL VID SIF MODE SEL switch: 1. SIF CHAL VID 5V/ 20V switch: 20V.	*f.* Observe oscilloscope. Measure pulse amplitude.	*f.* (1) Pulse amplitude is ± 20.0 v ± 4.0 v. (2) Pulse width is 0.80 µsec ± 0.05 µsec.	Malfunction 54 Malfunction 53
	MAIN TIME/ DIV switch: 50 µSEC.	SIF CHAL VID 5V/20V switch: 5V.	*g.* Disconnect cable from test set SIF CHAL VID CHAL VID OUT jack and connect to SIF CHAL VID PRE TRIG OUT jack.	*g.* None.	
	DELAYED TIME/DIV switch: .5 µSEC.		*h.* Observe oscilloscope. Adjust oscilloscope DIV DELAY control to observe pulse on B INPUT and measure puke amplitude and pulse width.	*h.* (1) Pulse present on B INPUT. (2) Pulse amplitude is +5.0 v ± 0.5 v. (3) Pulse width 0.8 µsec ± 0.1 µsec.	Malfunction 57 Malfunction 59 Malfunction 59
	DELAYED TIME/DIV switch: 50 µSEC. DISPLAY switch: ALT. MAIN TIME/ DIV switch: .2 MSEC.		*i.* Adjust oscilloscope DIV DELAY control to observe RDR TRIG OUT on A INPUT and SIF CHAL VID PRE TRIG OUT on B INPUT.	Pulse delay is 386.0 ± 0.5 µsec. NOTE Adjustable from 300.0 µsec to 395.0 µsec. This is nominal setting and may vary with different interrogator systems.	Malfunction 60
16			Mode 4 Challenge Output Test		
	DELAYED TIME/DIV switch: 20 µSEC.	PRT SEL (µSEC) switches: 0500.	*a.* Disconnect cable and 75 ohm termination between oscilloscope B INPUT and test set SIF CHAL VID PRE TRIG OUT jack.	*a.* None.	
			b. Connect oscilloscope B INPUT with 93 ohm termination and cable and other end of cable to test set MODE 4 CHAL VID OUT jack.	*b.* None.	

Table 3–3. Performance Test Procedure -Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3–4
16 (cont.)			*c.* Adjust oscilloscope DIV DELAY control to observe delay between pulse on A INPUT and first pulse on B INPUT.	*c.* (1) Pulse train present on B INPUT. (2) Nominal pulse delay is 182.5 µsec ± 0.6 µsec (actual tolerance beyond oscilloscope accuracy, for this test measure to 5.0 µsec). **NOTE** Adjustable from 172.0 µsec to 202.0 µsec. This is a nominal setting and may vary with different interrogator systems.	Malfunction 61 Malfunction 63
	MAIN TIME/DIV switch: 50 µSEC. DELAYED TIME/DIV switch: 10. µSEC. DISPLAY switch: B. B INPUT VOLTS/DIV switch: 2.		*d.* Adjust oscilloscope DIV DELAY control to observe complete pulse train on B INPUT.	*d.* Train consists of 36 evenly spaced pulses except pulse at fifth position is inhibited. (4 sync pulses, one blank pulse position, and 32 information pulses).	Malfunction 64
	DELAYED TIME/DIV switch: .1 µSEC.		*e.* Adjust oscilloscope DIV DELAY control to observe one pulse of train. Observe pulse amplitude and width of one pulse on B INPUT.	*e.* Pulse amplitude is 5.0 v + 0.5 v and width is 0.5 µsec ± 0.05 µsec.	Malfunction 65
17			Mode 4 GTC Trigger Output Test *a.* Remove cable from test set MODE 4 CHAL VID OUT jack and connect to MODE 4 GTC TRIG OUT jack.	*a.* None.	
	DISPLAY switch: ALT. MAIN TIME/DIV switch: .2 MSEC. DELAYED TIME/DIV switch: 50 µSEC. A INPUT VOLTS/DIV switch: 5.		*b.* Adjust oscilloscope DIV DELAY control to observe spacing between pulse on A and B INPUTS.	*b.* (1) Pulse present on B INPUT. (2) Nominal pulse spacing is 387.5 µsec ± 0.5 µsec nominal (actual tolerance beyond oscilloscope accuracy for this test measure to ± 25 µsec). **NOTE** Adjustable from 376.0 µsec to 406.0 µsec. This is a nominal setting and may vary with different interrogator systems.	Malfunction 66 Malfunction 68
	DELAYED TIME/DIV switch: .2 µSEC.		*c.* Adjust oscilloscope DIV DELAY control to view pulse on B INPUT.	*c.* None.	

Table 3-3. Perfomance Test Procedure—Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3-4
17 (cont.)	DISPLAY switch: B.		*d.* Observe pulse amplitude and width of pulse on B INPUT.	*d.* Pulse amplitude is 5.0 v ± 0.5 v and width is 0.80 µsec ± 0.02 µsec.	Malfunction 69
18			Decode Function Test		
	MAIN TIME/DIV switch: .1 MSEC. DELAYED TIME/DIV switch: 5 µSEC.	REPLIES MODULATION SEL switch: SIF.	*a.* Disconnect cable from test set MODE 4 GTC TRIG OUT jack and connect to REPLY VID OUT jack.	*a.* None.	
			b. Adjust oscilloscope DIV DELAY control to observe pulse train.	*b.* Reply pulse train present.	Malfunction 16
		TRIG SEL DCD MODE SEL switch: 1.	*c.* Observe oscilloscope and test set REPLIES REPLY INHIB indicator,	*c.* Reply disappears and REPLIES REPLY INHIB indicator lights.	Malfunction 70
			d. Press and hold test set BIT (MOM) switch for all of step 18.	*d.* Reply pulse train reappears and REPLIES REPLY INHIB indicator extinguishes.	Malfunction 71
		SIF CHAL VID SIF MODE SEL switch: 2.	*e.* Observe oscilloscope and test set REPLIES REPLY INHIB indicator.	*e.* Reply pulse train disappears and REPLIES REPLY INHIB indicator lights.	Malfunction 73
		TRIG SEL DCD MODE SEL switch: 2.	*f.* None.	*f.* Reply pulse train appears and indicator extinguishes.	Malfunction 74
		SIF CHAL VID SIF MODE SEL switch: 3/A.	*g.* Observe oscilloscope and test set REPLIES REPLY INHIB indicator.	*g.* Reply pulse train disappears and REPLIES REPLY INHIB indicator lights.	Malfunction 73
		TRIG SEL DCD MODE SEL switch: 3/A.	*h.* None.	*h.* Reply pulse train reappears and REPLIES REPLY INHIB indicator extinguishes.	Malfunction 74
		SIF CHAL VID SIF MODE SEL switch: C.	*i.* Observe oscilloscope and test set REPLIES REPLY INHIB indicator.	*i.* Reply pulse train disappears and REPLIES REPLY INHIB indicator lights.	Malfunction 73
		TRIG SEL DCD MODE SEL switch: C.	*j.* None.	*j.* Reply pulse train reappears and REPLY INHIB indicator extinguishes.	Malfunction 74
		SIF CHAL VID SIF MODE SEL switch: OFF. REPLIES MODULATION SEL switch: M4-3P.	*k.* Observe oscilloscope and test set REPLIES REPLY INHIB indicator.	*k.* Reply pulse train disappears and REPLIES REPLY INHIB indicator lights.	Malfunction 73

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Table 3-3. Performance Test Procedure-Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3-4
18 (cont.)		TRIG SEL DCD MODE SEL switch: 4.	*1.* None.	*l.* Three pulse reply appears and REPLIES REPLY INHIB indicator extinguishes.	Malfunction *75*
19			Timing Markers		
	Connect test set-up as shown in figure 3–21.		*a.* Observe four levels of markers.	*a.* Four levels of markers are present. (0.1, 1.0, 10.0 and 100.0 µsec ± 0.02%).	Malfunction 76
	MAIN TIME/DIV switch: *20* µSEC.		*b.* Adjust frequency counter C TRIGGER VOLTS control cw until steady reading is displayed.	*b.* Frequency counter indicates 10,000 KHz ± 2 KHz (0.1 µsec).	Malfunction 77
	DELAYED TIME/DIV switch: .1 µSEC. NOTE Frequency counter controls are set as follows: SENSITIVITY switch: FREQ C. C TRIGGER VOLTS switch: 1. Mode selector switch: SEP FUNCTION switch: FREQ. TIME base switch: 10^{2}.z C TRIGGER VOLTS control: ccw.		*c.* Measure on oscilloscope spacing from leading edge to leading edge of lowest amplitude level of markers.	*c.* (1) Markers are spaced 0.1 µsec apart. (2) Marker amplitude ≥ O.5 volts.	Malfunction 77 Malfunction 77
	DELAYED TIME/DIV switch: 1 µSEC.		*d.* Measure spacing from leading edge to leading edge of second level of markers.	*d.* Markers are spaced 1.0 µsec apart.	Malfunction 77
	DELAYED TIME/DIV switch: 10 µSEC.		*e.* Measure spacing from leading edge to leading edge of third level of markers.	*e.* Markers are spaced 10.0 µsec apart.	Malfunction 77
			f. Measure spacing from leading edge to leading edge of highest level of markers.	*f.* Markers are spaced 100.0 µsec apart.	Malfunction 77
20			External Gating		
	Connect test set-up as shown in figure 3- 19, except remove *75* termination from test set EXT GATE IN jack.	TRIG SEL DCD MODE SEL switch: OFF.	*a.* Adjust oscilloscope DIV DELAY control to observe reply pulse train.	*a.* Reply pulse train present.	

Table 3–3. Performance Test Procedure-Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3–4
20 (cont.)	Oscilloscope: MAIN EXT÷ 10/EXT/INT/ LINE switch: EXT. MAIN TIME/ DIV switch: 50 µSEC.		*b.* Attach 75 termination to test set EXT GATE IN.	*b.* Reply pulses disappear.	Malfunction 78
21	Connect test set-up as shown in figure 3–30. Oscilloscope B VOLTS/DIV switch: 2. MAIN TIME/ DIV switch: 2 µSEC. DELAYED TIME/DIV switch: .5 µSEC. DISPLAY switch: ALT. Set up pulse generator as follows: COARSE ATTN switch: 1. FINE ATTN control: midrange. PULSE NO. 2 switch: OUT. WIDTH switch: NAR. POLARITY switch: POS. SYNC switch: SYNC INT C. Set frequency counter as follows: FUNCTION switch: TIME B →C. Time base switch: 10^{-7}. COM/SEP switch: COM. B and C MULTIPLIER switches: 3.	REPLIES MODULA-TION SEL switch: OFF. TRIG SEL INT/DCD/ EXT switch: EXT. MEASURE-MENT FUNCTION SEL switch: PRF REPLY TRIG. MEASURE-MENT PRF RANGE switch: 1K.	External Trigger *a.* Adjust pulse generator BIAS control until pulses appear on oscilloscope. *b.* Adjust pulse generator FINE ATTN control until pulses on oscilloscope B INPUT are 5 volts in amplitude. c. Adjust oscilloscope DIV DELAY control to observe pulse on B INPUT. *d.* Adjust pulse generator WIDTH control until pulse width is 0.5 µsec on B INPUT. *e.* Adjust pulse generator RISE TIME control until pulse rise time is y50.1 µsec ON B INPUT. *f.* Adjust pulse generator PULSE RATE control for 500 µsec. g. Observe pulse on A INPUT,	*a.* None. *b.* None. *c.* None. *d.* None. *e.* None *f.* Test set MEASUREMENT meter indicates 2 KHz. *g.* Pulse present on A INPUT.	Malfunction 79 Malfunction 79

Table 3–3. Performance Test Procedure-Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3–4
21 (cont.)	B and C TRIGGER VOLTS switches: 0. B and C SLOPE switches: +.				
22			Input and Output Power Test		
	A INPUT VOLTS/DIV switch: *.5*. DISPLAY switch: A. MAIN TIME/DIV switch: *.5* MSEC. DELAYED TIME/DIV switch: 5 µSEC.	TRIG SEL INT/DCD/EXT switch: INT. TRIG SEL DCD MODE SEL switch: OFF. MEASUREMENT FUNCTION SEL switch: PWR. REPLIES MODULATION SEL switch: SIF.	a. Disconnect all video cables to test set and oscilloscope.	*a.* None.	
			b. Connect test set SUM RF IN/OUT jack to LOW PWR IN jack using 12 inch rf cable.	*b.* None.	
			c. Connect video cable from oscilloscope MAIN EXT INPUT to test set SCOPE TRIG *OUT.*	c. None.	
			d. Connect video cable from test set DEMOD VID OUT to oscilloscope A INPUT with *75* termination.	*d.* None.	
			e. Adjust test set MEASUREMENT DEMOD VID LEVEL control until MEASUREMENT meter indicates *30* dBw.	*e.* MEASUREMENT meter adjusts.	Malfunction 82
			f. Adjust oscilloscope DIV DELAY control to observe pulse train.	*f.* Pulse train present.	Malfunction 84
			g. Adjust test set MEASUREMENT DEMOD VID LEVEL control until video on oscilloscope A INPUT is 1.0 volt.	*g.* None.	
			h. Observe power indication on test set MEASUREMENT meter.	*h.* Power indication is 28.0 to 32.0 dBW. CAUTION During this test the power level out of test set SUM RF IN/OUT jack is 0.0 ± 1.0 dBm. See figure 3–2 for meter conversion information for testing with the LOW PWR IN jack. Damage to the test set can occur if an input to the LOW PWR IN jack exceeds +20 dBm (1/10 watt).	Malfunction 97
			i. Disconnect cable from test set SUM RF IN/OUT jack and connect to DIFF RF IN/OUT jack. Adjust test MEASUREMENT DEMOD VID LEVEL control until video on oscilloscope A INPUT is 1.0 volts.	Pulse train present.	Malfunction 99

Table 3-3. Performance Test Procedure-Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3-4
22 (cont.)			*j.* Observe power indication on test set MEASUREMENT meter.	i. Power indication is 28.0 to 32.0 dBW. **CAUTION** During this test the power level out of the test set SUM RF IN/OUT jack is 0.0 ± 1.0 dBm. See figure 3-2, meter conversion information for testing the LOW PWR IN jack. Damage to the test set can occur if an input to the LOW PWR IN jack exceeds ± 20 dBm (1/10 watt).	Malfunction 106
23			Reply Interleave Test		
		SIG GEN NORM/INTER-LEAVE switch INTER-LEAVE	*a.* Observe oscilloscope.	*a.* Signal disappears.	Malfunction 108
	MAIN TIME/DIV switch: 50 µSEC.		*b.* Disconnect cable from test set DIFF RF IN/OUT jack and connect to SUM RF IN/OUT jack.	*b.* None.	
			c. Adjust oscilloscope DIV DELAY to observe interleaved reply.	*c.* Interleaved reply is displayed.	Malfunction 109
	DELAYED TIME/DIV switch:.1 µSEC.		*d.* Adjust oscilloscope DIV DELAY control to observe interleaved pulse trains and measure spacing between first and second pulse.	*d.* Pulse spacing is 0.70 µsec ± 0.05 µsec.	Malfunction 113
24			External Modulation		
	Connect test set-up as shown in figure 3-20.	REPLIES MODULATION SEL switch.	*a.* Adjust pulse generator BIAS control until pulse appears on oscilloscope.	*a.* None.	
	Oscilloscope: DELAYED TIME/DIV switch: .5 MSEC.	OFF. SIG GEN NORM/INTER-LEAVE switch: NORM.	*b.* Adjust pulse generator FINE ATTN control until pulse on oscilloscope A INPUT is 5 volts in amplitude.	*b.* None.	
	MAIN TIME/DIV switch: 2 MSEC.		*c.* Adjust oscilloscope DIV DELAY control to observe pulse.	*c.* None.	
	A INPUT VOLTS/DIV switch: 2.		*d.* Adjust pulse generator WIDTH control until pulse width is 0.5 µsec.	*d.* None.	
	Set up pulse generator as follows:		*e.* Adjust pulse generator RISE TIME control until pulse rise time is ≤ 0.1 µsec.	*e.* None.	

Table 3–3. Performance Test Procedure—Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal see table 3–4
24 (cont.)	COARSE ATTN switch: 1. FINE ATTN control: midrange, PULSE NO. 2 switch: OUT. WIDTH switch: NAR. POLARITY switch: POS. SYNC switch: EXT GOING+. B VOLTS/DIV switch: .5. DISPLAY switch: ALT. DELAYED TIME/DIV switch: .1 µSEC.		*f.* Adjust test set DEMOD VID LEVEL control until pulse on B INPUT is 1.0 volt in amplitude.	*f.* One pulse present on B INPUT for each pulse on A INPUT.	Malfunction 114
			g. Adjust oscilloscope DIV DELAY control to observe one pulse on A INPUT and one pulse on B INPUT and measure delay.	*g.* Delay is ≤ 0.3 µsec.	Malfunction 115
25			Swept RF Test		
	Connect test set-up as shown in figure 3–24. MAIN TIME/DIV switch: .5 MSEC. DELAYED TIME/DIV switch: .2 MSEC.	SIG GEN FUNCTION switch: SWP ± 5 MHZ.	*a.* Adjust oscilloscope DIV DELAY control to observe five markers on A INPUT.	*a.* Five positive markers present.	Malfunction 116
		SIG GEN FUNCTION switch: SWP ± 15 MHZ.	*b.* Adjust oscilloscope DIV DELAY control to observe nine markers on B INPUT.	*b.* Nine positive markers present.	Malfunction 119
	B VOLTS/DIV switch: 2. DELAYED TIME/DIV switch: 50 µSEC.	SIG GEN FUNCTION switch: SWP ± 5 MHZ. MEASUREMENT FUNCTION SEL switch: FREQ. BIT (MOM) switch: press and hold.	*c.* Adjust oscilloscope DIV DELAY control to observe five markers on B INPUT and frequency signal on A INPUT.	*c.* None.	
			d. Interpolate frequency of peak of signal on B INPUT by using frequency markers on A INPUT.	*d.* Frequency of peak of signal on A INPUT is within ± 0.3 MHz of center frequency marker on B INPUT.	Malfunction 120

Table 3–4. Troubleshooting Procedure

Malfunction	Fault isolation procedures and probable causes	Corrective action
1. POWER 1.5 AMP fuseholder lights when POWER ON/OFF switch is set to ON.	*a.* Defective POWER 1.5 AMP fuse F1. **CAUTION** If fuse faults after being replaced, isolate short in power circuit before proceeding. Isolate using continuity check (fig. FO-19).	*a.* Replace fuse (refer to TM 11–6625–2610–12).
	b. Defective power supply PSI.	*b.* Replace power supply PSI (para 3–8g and *3–9a).*
	c. Defective connector PS1J1 or P1. Isolate using continuity check (fig. FO–19 and FO–20).	*c.* Replace connector.
	d. Defective fuseholder XF1.	*d.* Replace fuseholder XF1 (para 3–8f and 3–9b).
	e. Defective POWER indicator housing XDS2.	*e.* Replace POWER indicator housing XDS2 (para 3–8f and 3–9b).
2. POWER indicator does not light when POWER ON/OFF switch is set to ON.	*a.* Defective POWER indicator DS2.	*a.* Replace POWER indicator lamp. (Refer to TM 11–6625–2610–12).
	b. Defective POWER indicator housing XDS2.	*b.* Replace housing XDS2 (para 3–8f and 3–9b).
	c. Defective POWER ON/OFF switch S21. Isolate using continuity check (fig. FO–19)	*c.* Replace switch S21 (para 3–8f and 3–9b).
	d. Defective POWER connector J1. Isolate using continuity check (fig. FO–19).	*d.* Replace jack J1 (para 3-8f and 3–9b).
	e. Defective power cable.	*e.* Replace power cable.
3. DC FAULT Indicator illuminates when POWER ON/OFF switch is set to ON.	*a.* Using differential voltmeter, check voltage between PS1A1TP1 (+) and GND (-). Voltage should be +27.75 to 28.25 volts. If abnormal, proceed to malfunction 4. If normal proceed to step *b.*	*a.* None.
	b. Using differential voltmeter, check voltage between PS1A1TP5 (+) and GND (-). Voltage should be 11.75 to +12.25 volts. If abnormal, proceed to malfunction 5. If normal, proceed to step c.	*b.* None.
	c. Using differential voltmeter, check voltage between PS1A1TP6 (-) and GND (+). Voltage should be -11.75 to -12.25 volts. If abnormal, proceed to malfunction 6. If normal, proceed to step d.	*c.* None.
	d. Using differential voltmeter, check voltage between PS1A1TP7 (+) and GND (-). Voltage should be +4.75 to +5.05 volts. If abnormal, proceed to malfunction 7. If normal, de fault circuit is misadjusted or circuit card PS1 is defective.	*d.* (1) Adjust (para 3-10b). (2) Replace power supply PS1 (para 3–8g and 3–9a). (3) Performance test (table 3-8).
4. Improper or no voltage at PS1A1TP1, +28 volt power supply.	*a.* +28 volt improperly adjusted.	*a.* Adjust power supply (para 3–10b)
	b. Defective circuit card PS1A1.	*b.* (1) Replace power supply PS1 (para 3–8g and 3–9a). (2) Adjust power supply (para 3-10 b).
	c. Defective power supply PS1.	(1) Replace power supply PS1 (para 3–8g and 3–9a). (2) Adjust (para *3–10b).*

Table 3-4. Troubleshooting Procedure—Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
24. (cont.)	*d.* Improper load on +28 volt power supply.	*d.* Check resistance between P1–S and ground with power supply disconnected. Locate actual short by disconnecting circuit cards and assemblies until short no longer exists, then replace defective assembly.
5. +12 volt power supply improper voltage.	*a.* +12 volt regulator improperly adjusted.	*a.* Adjust power supply (para 3– 10b).
	b. Defective circuit card PS1A1.	*b.* (1) Replace power supply PS1 (para 3–8g and 3–9a). (2) Adjust power supply (para 3-10b).
	c. Defective power supply PSI.	*c.* (1) Replace power supply PS1 (para 3–8g and 3–9a). (2) Adjust (para *3–10b).*
	d. Improper load on +12 volt power supply.	*d.* Check resistance between P1–D and ground with power supply disconnected. Isolate short (malfunction *4d* above).
6. -12 volt power supply improper voltage.	*a.* -12 volt regulator improperly adjusted.	*a.* Adjust power supply (para *3–10b).*
	b. Defective circuit card PS1A1.	*b.* (1) Replace power supply PS1 (para 3–8g and 3–9a). (2) Adjust power supply (para 3-10b).
	c. Defective power supply PS1.	*c.* (1) Replace power supply PS1 (para 3–8g and 3–9a). (2) Adjust (para 3–10b).
	d. Improper load on *-12* volt power supply.	*d.* Check resistance between P1–H and ground with power supply disconnected. Isolate short (malfunction 4d above).
7. +5 volt power supply improper voltage.	*a.* +5 volt regulator improperly adjusted.	*a.* Adjust power supply (para 3–10b).
	b. Defective circuit card PS1A1.	*b. (1)* Replace power supply PS1 (para 3–8g and 3–9a). *(2)* Adjust power supply (para 3–10b).
	c. Improper load.	*c.* Check resistance between P1–L and ground with power supply disconnected and locate short circuit (para *4d* above).
	d. Defective power supply PS1.	*d.* Replace power supply PS1 (para 3–8g and 3–9a).
8. POWER DC FAULT indicator does not light when activated.	*a.* Defective POWER DC FAULT indicator DS1.	*a.* Replace DC FAULT indicator DS1 lamp, refer to TM 11–6625–2610–12.
	b. Defective POWER DC FAULT indicator housing XDS1.	*b.* Replace DC FAULT indicator housing XDS1 (para 3–8a and 3–9g).
	c. Defective circuit card PS1A1. Check for +28 volts at PS1A1Q1–C.	*c.* (1) Replace power supply PS1 (para 3–8g and *3–9a).* (2) Adjust (para 3–10b).
	d. Defective power supply PSI	*d.* Replace power supply PS1 (para 3–8g and 3–9a).
9. No prf indication on MEASUREMENT MENT meter or indication is out of tolerance. a. No meter indication on any of the positions of MEASUREMENT PRF RANGE switch.	*a.* Check prf count trig at TPD8 for both waveform and prf (use frequency counter for prf). If abnormal, proceed to malfunction	

Table 3-4. Troubleshooting Procedure—Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
9. (cont.)	10. If normal, fault is one of the following: defective circuit card A10, defective meter M1, or defective MEASUREMENT FUNCTION SEL switch S31 or defective MEASUREMENT PRF RANGE switch S32.	
	Probable Causes	
	(1) Defective circuit card A10.	(1) (a) Replace circuit card A10 (para *3-8q* and 3-9q). (b) Calibrate (para 3-10h).
	(2) Defective MEASUREMENT meter Ml. Hint to check meter: Set MEASUREMENT FUNCITON SEL switch S31 to PWR. If meter indication follows variation of MEASUREMENT DEMOD VID LEVEL control, meter is probably operating.	(2) (a) Replace MEASUREMENTS meter M1 (para 3-8f and *3-9 b).* (b) Adjust (para 3-10g).
	(3) Defective MEASUREMENT FUNCTION SEL switch S31. Isolate by continuity check (fig. FO-19).	(3) Replace MEASUREMENT FUNCTION SEL switch S31 (para 3-8f and *3-9b).*
	(4) Defective MEASUREMENT PRF RANGE switch S32. Isolate by continuity check (fig. FO-19).	(4) Replace MEASUREMENT FUNCTION SEL switch S32 (para *3-8f* and *3-9b).*
b. Meter indication is out of tolerance for only one setting of PRT SEL (µSEC) in table 3-3, step *2b.*	*b.* Fault is one of the following: (1) Defective circuit card Al.	*b.* (1) (a) Replace circuit card A1 (para 3-8q and *3-9q).* (b) Adjust (para 3-100.
	(2) Defective PRT SEL (µSEC) switches S5 through S8. Isolate by continuity check (fig. FO-19).	(2) Replace faulty switch (para 3-8f and *3-9b).*
	c. Measurement section is out of adjustment.	*c.* Calibrate per para 3- 10g.
10. No prf count trig at TPD8.	Check ZERO TRIG at TPA2. If abnormal, proceed to malfunction 11. If normal, circuit card A9 or MEASUREMENT FUNCTION SEL switch S31 is defective.	
	Probable Cause	
	a. Defective circuit A9.	*a.* (1) Replace circuit card A9 para *3-8q* and *3-9q).* (2) Adjust (para 3-10e).
	b. Defective MEASUREMENT FUNCTION SEL switch S31. Isolate by continuity check (fig. FO-19).	*b.* Replace MEASUREMENT FUNCTION SELECT switch (para *3-8f* and *3-9b).*
11. Abnormal ZERO TRIG at TPA2.	*a.* Defective circuit card A1.	*a.* (1) Replace circuit card A1 (para 3-8q and *3-9q).* (2) Adjust circuit card A1 (para 3-10i).
	b. Defective circuit card A2.	*b.* Replace circuit card A2 (para *3-8q* and *3-9q).*
	c. Defective TRIG SEL INT/DCD/EXT switch S24. Isolate by continuity check (fig. FO-19).	*c.* Replace TRIG SEL INT/DCD/EXT switch S24 (para *3-8f* and *3-9b).*
12. No signal at SCOPE TRIG OUT jack.	Check zero trigger at TPA2. If abnormal refer to malfunction 13. If normal, fault is one of the following	
	a. Defective circuit card A3.	*a.* (1) Replace circuit card A3 (para *3-8q* and *3-9q).*

Table 3–4. Troubleshooting Procedure–Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
12. (cont.)		(2) Adjust circuit card A3 (para 3–10c and *d).*
	b. Defective SCOPE TRIG OUT jack J3,	*b.* Replace faulty J3 (para 3–8f and *3–9b).*
13. Abnormal signal at TPA2.	*a.* Defective circuit card A2.	*a.* Replace circuit card A2 (para 3–8q and *3–9q).*
	b. Defective circuit card A1.	*b.* (1) Replace circuit card A1 (para *3–8q* and *3–9q).* *(2)* Adjust circuit card A1 (para 3–10i).
14. Pulse at SCOPE TRIG OUT jack amplitude or width out of tolerance.	Defective circuit card A3.	*a.* Replace circuit card A3 (para *3–8q* and *3–9q).* *b.* Adjust circuit card A3 (para 3–10C and *d).*
15. No signal at RDR TRIG OUT jack or signal is out of tolerance.	a. Defective circuit card A3.	*a.* (1) Replace circuit card A3 (para *3–8q* and *3–9q).* *(2)* Adjust circuit card A3 (para 3–10C and *d).*
	b. Defective RDR TRIG OUT jack J4.	*b.* Replace RDR TRIG OUT jack J4 (para 3–8f and *3–9b).*
16. No REPLY VID OUT signal but REPLIES REPLY INHIB indicator is extinguished.	Check main mod signal at TPD6. If abnormal, refer to malfunction 17. If normal, fault is one of the following.	
	a. Defective circuit card A9.	*a.* (1) Replace circuit card A9 (para *3-8q* and *3–9q).* *(2)* Adjust (para 3–10e *(2)(a)* through (ac)).
	b. Defective jack J6.	*b.* Replace REPLIES REPLY VID OUT jack J6 (para 3–8f and *3-9 b).*
17. Abnormal signal at TPD6.	Check reply triggers out TPD3. If abnormal refer to malfunction 20. If normal refer to malfunction 18.	
18. Normal signal at TPD3	Check pos gate at TPF7, If normal refer to malfunction 19. If abnormal, fault is one of the following:	
	a. Defective rf generator All.	*a.* (1) Replace rf generator All (para *3-8b* and 3-9A. (2) Adjust rf generator All (para 3–10f).
	b. Defective SIG GEN FUNCTION switch S23. Isolate by continuity check (fig. FO–19).	*b.* Replace faulty switch S23 (para 3–8f and para *3–9b).*
19. Normal signal at TPF7	*a.* Defective circuit card A9.	*a.* (1) Replace circuit card A9 (para 3–8q and *3-9q).* (2) Adjust circuit card A9 (para 3–10e *(2)(a)* through (ac)).
	b. Defective circuit card A4.	*b.* Replace circuit card A4 (para *3–8q* and 3–9q).
	c. Defective circuit card A3	*c.* (1) Replace circuit card A3 (para 3–8q and *3–9q).* (2) Adjust circuit card A3 (para 3-10C and *d).*

Table 3-4. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
19. (cont.)	*d.* Defective REPLIES MODULATION SEL switch S20. Isolate by continuity check (fig. FO-19).	*d.* Replace faulty switch S20 (para 3-8f and *3–9b).*
	e. Defective EXT GATE IN jack J?. Check continuity for short.	*e.* Replace EXT GATE IN jack J7 (para 3–8f and *3–9b).*
	f. Defective REPLIES GATING PASS and INHIB switches S13 through S16. Isolate by continuity check (fig. FO-19).	*f.* Replace faulty switch (para 3-8f and *3–9b).*
20. Abnormal signal at TPD3.	Check delayed reply trigger signal at TPB8. If abnormal refer to malfunction 21. If normal fault is one of the following:	
	a. Defective circuit card A7.	*a.* Replace circuit card A7 (para *3–8q* and 3–9q).
	b. Defective circuit card A8.	*b.* Replace circuit card A8 (para *3–8q* and *3–9q).*
21. Abnormal signal at TPB8.	Check reply trig signal at TPB1. If abnormal refer to malfunction 22. If normal, fault is one of the following:	
	a. Defective circuit card A4.	*a.* Replace circuit card A4 (para *3–8q* and *3–9q).*
	b. Defective REPLIES RANGE DELAY SEL switches S9 through S12. Isolate by continuity check (fig. FO–19).	*b.* Replace faulty switch (para *3–8f* and *(3-9b).*
22. Abnormal signal at TPB1.	Check SIF gate signal at TPA5 and SIF clock signal at TPA7. If either is abnormal refer to malfunction 23. If both are normal circuit card A2 is defective.	Replace circuit card A2 (para 3–8q and 3–9q).
23. Abnormal signals at TPA5 or TPA7.	*a.* Defective circuit card Al.	*a.* (1) Adjust circuit card Al (para 3-10i. (2) If unable to adjust replace circuit card A1 (para 3-8q and 3–9q). (3) Adjust circuit card Al (para 3-10i
	b. Defective circuit card A2.	*b.* Replace circuit card A2 (para 3–8q and 3–9q),
24. Improper delay from RDR TRIG OUT jack to REPLY VID OUT jack.	Check reply trigger at TPB1. If abnormal, refer to malfunction 25. If normal, fault is one of the following.	
	a. Defective circuit card A4.	*a.* Replace circuit card A4 (para 3–8q and 3–9q).
	b. Defective RANGE DELAY SEL switches S9 through S12. Isolate by continuity check (fig. FO–19).	*b* Replace faulty switch (para 3–8f and 3–9b).
25. Abnormal delay at TPB1.	Check SIF gate at TPA5 and SIF clock at TPA7. If abnormal refer to malfunction 23. If normal replace circuit card A2.	Replace circuit card A2 (para 3–8q and 3–9q).
26. Improper ratio of radar triggers to reply pulse trains.	*a.* Defective circuit card A4.	*a.* Replace circuit card A4 (para 3–8q and 3–9q).
	b. Defective REPLIES GATING PASS or INHIB switches S13 through S16. Isolate by continuity, check (fig. FO–19).	*b.* Replace faulty switch (para 3–8f and 3–9b).

Table 3-4. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
27. No meter indication.	a. Defective circuit card A9.	a. (1) Replace circuit card A9 (para 3-8q and *3-9q).* (2) Adjust circuit card A9 (para 3-10e (2)(a) thru (ac).
	b. Defective terminal board TB2.	b. Replace terminal board TB2 (para 3-8f and *3-9b).*
	c. Defective MEASUREMENT 75 Ω/2K Ω switch S28.	c. Replace faulty switch S28 (para 3-8f and *3-9b).*
	d. Defective MEASUREMENT FUNCTION SEL switch S31.	d. Replace faulty switch S31 (para 3-8f and *3-9b).*
	e. Defective MEASUREMENT EXT VID IN jack J9.	e. Replace jack J9 (para 3-8f and *3-9b).*
28. Improper delay from radar trigger to reply pulse train.	a. Defective circuit card A4.	a. Replace circuit card A4 (para *3-8q* and and *3-9q).*
	b. Defective REPLIES RANGE DELAY SEL switches S9 through S12. Isolate by continuity, check (fig. FO-19).	b. Replace faulty switch (para 3-8f and *3-9b).*
29. Improper amplitude at REPLY VID OUT jack J6.	Defective circuit card A9.	a. Replace circuit card A9 (para *3-8q* and *3-9q).* b. Adjust circuit card A9 (para 3-10e (2)(a) thru (ac).
30. Improper code at REPLIES REPLY VID OUT jack J6.	a. Defective circuit card A8.	a. Replace circuit card A8 (para *3-8q* and *3-9q).*
	b. Defective REPLIES SIF REPLY CODE switches S1 through S4. Isolate by continuity, check (fig. FO-19).	b. Replace faulty switch (para 3-8f and *3-9b).*
	c. Defective REPLIES MODULATION SEL switch S20. Isolate by continuity, check (fig. FO-19).	c. Replace faulty switch S20 (para 3-8f and *3-9b).*
31. Reply pulse width out of tolerance.	a. Circuit card A9 out of adjustment.	a. Adjust circuit card A9 (para 3-10e *(2)(a)* through (ac).
	b. Defective circuit card A9.	b. (1) Replace circuit card A9 (para *3-8q* and *3-9q).* (2) Adjust circuit card A9 (para 3-10e (2)(a) through (ac).
	c. Defective REPLIES REPLY WIDTH SELECT switch S18. Isolate using continuity check (fig. FO-19).	c. Replace faulty switch S18 (para 3-8f and *3-9b).*
32. Improper spacing between bracket pulses.	Defective circuit card A8.	Replace circuit card A8 (para *3-8q* and *3-9q).*
33. Incorrect number of pulses.	a. Defective circuit card A8.	a. Replace circuit card A8 (para *3-8q* and *3-9q).*
	b. Defective circuit card A7.	b. Replace circuit card A7 (para *3-8q* and *3-9q).*
	c. Defective REPLIES SUB PULSE SEL switch S19. Isolate using continuity check (fig. FO-19).	c. Replace faulty switch S19 (para 3-8f and *3-9b).*
	d. Defective REPLIES SUB PULSE POS switch S22. Isolate using continuity check (fig. FO-19).	d. Replace faulty switch S22 (para 3-8f and 3-9b).

Table 3-4. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
33. (cont.)	e. Defective REPLIES SIF REPLY CODE switches S1 through S4. Isolate using continuity, check (fig. FO- 19).	e. Replace faulty switch (para 3-8f and *3–9b).*
34. Vary SIF reply substitute pulse out of tolerance.	*a.* Circuit card A9 out of adjustment.	*a.* Adjust circuit card A9 (para *3–10e (2)(a)* through (ac).
	b. Defective circuit card A9.	*b. (1)* Replace circuit card A9 (para 3-8q and *3-9q).* (2) Adjust circuit card A9 (para 3–10e (2)(a) through (ac).
35. Vary SIF reply substitute pulse width vary out of tolerance.	Defective REPLIES REPLY WIDTH VARY control (RIB).	Replace faulty switch S18 (para 3–8f and *3-9b).*
36. Improper substitute pulse position,	*a.* Defective circuit card A7.	*a.* Replace circuit card A7 (para 3-8f and *3–9b).*
	b. Defective circuit card A8.	*b.* Replace circuit card A8 (para 3–8q and 3–9q).
	c. Defective REPLIES SUB PULSE SEL switch S19. Isolate using continuity, check (fig. FO-19).	c. Replace faulty switch S19 (para *3–8f* and *3–9b).*
37. No mode 4 reply pulses.	Check M4 reply and sub pulse signal at TPC10. If abnormal refer to malfunction 38. If normal, defective circuit card A8.	Replace circuit card A8 (para *3–8q* and *3-9q).*
38. Abnormal signal at TPC10	Check mode 4 F.T. signal at TPC6. If abnormal refer to malfunction 39. If normal, defective circuit card A7.	Replace circuit card A7 (para *3–8q* and *3-9q).*
39. Abnormal signal at TPC6.	Check mode 4 enable signal at TPB1O. If normal refer to malfunction 40. If abnormal, fault is one of the following *a.* Defective circuit card A5.	*a.* Replace circuit card A5 (para *3-8q* and 3–9q).
	b. Defective REPLIES MODULATION SEL switch S20. Isolate by continuity, check (fig. FO-19).	*b.* Replace faulty switch S20 (para 3-8f and *3–9b).*
40. Normal signal at TPB1O	Check M4 shift clock at TPC9. If abnormal refer to malfunction 41. If normal, defective circuit card A6.	Replace circuit card A6 (para 3-8q and *3–9q).*
41. Abnormal signal at TPC9	*a.* Defective circuit card A7.	*a.* Replace circuit card A7 (para *3–8q* and 3-9q).
	b. Defective circuit card A2.	*b.* Replace circuit card A2 (para *3–8q* and 3-9q).
42. Mode 4 reply spacing out of tolerance.	Defective circuit card A7.	Replace circuit card A7 (para 3-8q and 3-9q).
43. Mode 4 reply substitute pulse spacing out of tolerance.	*a.* Defective circuit card A7.	a. Replace circuit card A7 (para 3-8q and 3–9q).
	b. Defective REPLIES SUB PULSE SEL switch S19. Isolate by continuity, check (fig. FO-19).	*b.* Replace faulty switch S19 (para *3–8f* and *3–9b).*
44. Mode 4 one pulse reply missing.	*a.* Defective circuit card A7.	*a.* Replace circuit card A7 (para *3-8q* and 3–9q).

Table 3-4. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
44. (cont.)	*b.* Defective REPLIES MODULATION SEL switch S20. Isolate by continuity check (fig. FO-19).	*b.* Replace faulty switch S20 (para *3-8f* and *3-9 b).*
45. Improper jamming operation mode 4.	Check gated jamming triggers at TPC5. If abnormal, refer to malfunction 46. If normal, circuit card A8 is defective.	Replace circuit card A8 (Para 3-89 and 3-9q).
46. Abnormal jamming trigger at TPC5.	Check jamming triggers at TPD1. If abnormal refer to malfunction 47. If normal, fault is one of the following.	
	a. Defective circuit card A6.	*a.* Replace circuit card A6 (para 3-8q and *3–9q).*
	b. Defective REPLIES M4 JAMMING switch S17. Isolate using continuity check (fig. FO-19).	*b.* Replace switch S17 (para 3-8f and *3–9b).*
47. Abnormal jamming trigger at TPD1	Defective circuit card A7.	Replace circuit card A7 (para *3-8q* and *3–9q).*
48. Improper I/P or EMERG operation.	a. Defective circuit card A8.	*a.* Replace circuit card A8 (para *3-8q* and *3–9q).*
	b. Defective REPLIES MODULATION SEL switch S20. Isolate using continuity check (fig. FO-19).	*b.* Replace switch S20 (para 3–8f and *3–9b).*
49. Improper garble operation.	a. Defective circuit card A7.	*a.* Replace circuit card A7 (para *3-8q* and 3–9q).
	b. Defective circuit card A6.	*b.* Replace circuit card A6 (para *3–8q* and *3–9q).*
	c. Defective REPLIES MODULATION SEL switch S20. Isolate by continuity check (fig. FO-19).	c. Replace switch S20 (para 3–8f and *3–9b).*
50. Improper 30 KHz operation.	Check M4 chal at TPA10 for 500 KHz signal. If abnormal refer to malfunction 51. If normal, fault is one of the following:	
	a. Defective circuit card A9.	*a. (1)* Replace circuit card A9 (para *3–8q* and *3–9q).* (2) Adjust (para 3–10e (2)(a) through (ac).
	b. Defective REPLIES MODULATION SEL switch S20. Isolate by continuity check (fig. FO-19).	*b.* Replace switch S20 (para 3–8f and *3–9b).*
51. Abnormal signal at TPA10.	Defective circuit card A2	Replace circuit card A2 (para 3–89 and *3–9q).*
52. No SIF challenge video pulses.	Check SIF chal triggers at TPB3. If abnormal refer to malfunction 53. If normal, fault is one of the following:	
	a. Defective circuit card A3.	a. (1) Replace circuit card A3 (para 3–89 and *3–9q).* (2) Adjust circuit card A3 (para 3–10C and *d).*
	b. Defective SIF CHAL VID 5V/20V switch S26. Isolate by continuity check (fig. FO–19).	b. Replace faulty switch S26 (para 3–8f and 3–9b).

Table 3-4. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
52. (cont.)	*c.* Defective SIF CHAL VID OUT jack J18.	c. Replace faulty jack J18 (para 3-8f and *3–9b).*
53. Abnormal signal at TPB3	*a.* Defective circuit card A2.	*a.* Replace circuit card *A2* (para *3–8q* and *3–9q).*
	b. Defective SIF CHAL VID SIF MODE SEL switch S25. Isolate by continuity check (fig. FO-19).	*b.* Replace faulty switch S25 (para 3–8f and *3–9b).*
54. Improper SIF challenge video pulse amplitude.	*a.* Defective circuit card A3.	*a.* (1) Replace circuit card A3 (para *3–8q* and *3–9q).* *(2)* Adjust circuit card A3 (para 3-1Oc and *d).*
	b. Defective SIF CHAL VID 5V/20V switch S26. Isolate by continuity check (fig. FO–19).	*b.* Replace faulty switch S26 (para 3–8f and 3–9b).
55. Improper SIF challenge video pulse width	Defective circuit card A3.	*a.* Adjust circuit card A3 (para 3–10e and *d).* *b.* (1) Replace circuit card A3 (para 3-8q and *3–9q).* *(2)* Adjust circuit card A3 (para 3-1Oc and *d).*
56. Improper SIF challenge video pulse spacing.	Defective circuit card A2.	Replace circuit card A2 (para *3–8q* and *3–9q).*
57. No pulse at SIF CHAL VID PRE TRIG OUT jack.	Check SIF pre trigger signal at TPA4. If abnormal refer to malfunction 58. If normal, fault is one of the following:	
	a. Defective circuit card A3.	*a.* (1) Replace circuit card A3 (para *3–8q* and *3–9q).* *(2)* Adjust circuit card A3 (para 3–10c and *d).*
	b. Defective SIF CHAL VID PRE TRIG OUT jack J19. Isolate by continuity check (fig. FO–19).	*b.* Replace faulty jack J19 (para 3–8f and 3–9b).
58. Abnormal signal at TPA4.	Defective circuit card A1.	*a.* Replace circuit card Al (para *3–8q* and *3–9q).* *b.* Adjust circuit card Al (para 3–10i).
59. Pre trigger pulse width or amplitude out of tolerance.	Defective circuit card A3.	*a.* Replace circuit card A3 (para 3–8q and and *3-9q).* *b.* Adjust circuit card A3 (para 3–10c and *d).*
60. Improper pre trigger delay.	Defective circuit card A1.	*a.* Adjust circuit card Al (para 3–10i). *b.* If unable to adjust, replace circuit card Al (para 3–8q and *3–9q).* *c.* Adjust circuit card A1 (para 3–10c and *d).*
61. No mode 4 challenge pulses.	Check mode 4 composite signal at TPA10. If abnormal refer to malfunction 62. If normal fault is one of the following:	
	a. Defective circuit card A3.	*a.* (1) Replace circuit card A3 (para 3–8q and 3–9g).

Table 3-4. Troubleshooting Procedure–Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
61. (cont.)		(2) Adjust circuit card A3 (para 3-10c and *d*).
	b. Defective MODE 4 CHAL VID OUT jack J11.	*b.* Replace faulty jack J11 (para 3–8f and *3–9b*).
62. Abnormal signal at TPA10.	Defective circuit card A2.	Replace circuit card A2 (para *3–8q* and *3-9q*).
63. Improper Mode 4 delay.	*a.* Defective circuit card A1.	*a.* (1) Adjust circuit card A1 (para 3-10i. (2) If unable to adjust, replace circuit card A1 (para *3–8q* and *3–9q*). (3) Adjust circuit card A1 (para 3-100.
	b. Defective circuit card A2.	*b.* Replace circuit card A2 (para *3–8q* and *3–9q*).
64. Mode 4 challenge pulse train spacing out of tolerance or ISLS pulse present.	*a.* Defective circuit card A2.	*a.* Replace circuit card A2 (para *3-8q* and *3–9q*).
	b. Defective circuit card A3.	*b.* (1) Replace circuit card A3 (para 3–8q and *3–9q*). (2) Adjust circuit card A3 (para 3–10c and *d*).
65. Mode 4 challenge pulse train amplitude or width out of tolerance.	Defective circuit card A3.	*a.* Replace circuit card A3 (para *3–8q* and *3–9q*).
		b. Adjust circuit card A3 (para 3–10c and *d*).
66. No mode 4 GTC pulse.	Check Mode 4 composite signal at TPA10. If abnormal refer to malfunction 67. If normal, fault is one of the following:	
	a. Defective circuit card A3	*a.* (1) Replace circuit card A3 (para 3-8q and *3–9q*). (2) Adjust circuit card A3 (para 3–1c and *d*).
	b. Defective MODE 4 GTC TRIG OUT jack J15.	*b.* Replace faulty jack J15 (para 3–8f and *3–9b*).
67. Abnormal signal at TPA10.	*a.* Defective circuit card A2.	*a.* Replace circuit card A2 (para *3–8q* and *3–9q*).
	b. Defective circuit card A1.	*b.* (1) Replace circuit card A1 (para *3–8q* and *3–9q*). (2) Adjust circuit card Al (para 3–10i).
68. Improper mode 4 GTC trigger delay,	*a.* Defective circuit card A1.	*a.* (1) Adjust circuit card Al (para 3–10i). (2) If unable to adjust, replace circuit card A1 (para *3–8q* and *3–9q*). (3) Adjust circuit card Al (para 3-10i).
	b. Defective circuit card A2.	*b.* Replace circuit card A2 (para *3–8q* and *3–9q*).
69. Mode 4 GTC trigger pulse amplitude or width out of tolerance.	Defective circuit card A3.	*a.* Replace circuit card A3 (para 3–8q and *3–9q*). *b.* Adjust circuit card A3 (para 3–10c and *d*).
70. Reply pulse train present and REPLIES REPLY INHIB indicator extinguished.	Defective TRIG SEL DCD MODE SEL switch S27, Isolate by continuity check (fig. FO–19).	Replace faulty switch S27 (para 3–8f and *3–9b*).

Table 3-4. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
71. Reply pulse train not present and REPLIES REPLY INHIB indicator lights.	Check decode trigger at TPC1. If abnormal refer to malfunction 72. If normal, defective circuit card A2.	Replace circuit card A2 (para *3-8q* and *3–9q).*
72. Abnormal signal at TPC1.	*a.* Defective circuit card A5.	*a.* Replace circuit card A5 (para 3–8q and 3–9q).
	b. Defective BIT (MOM) switch S37. Isolate by continuity check (fig. FO–19).	*b.* Replace faulty switch S37 (per para 3–8f and *3–9b).*
73. Reply pulse train present and REPLIES REPLY INHIB indicator extinguished.	Defective circuit card A5.	Replace circuit card A5 (para 3–8q and *3–9q).*
74, Reply pulse train not present and REPLIES REPLY INHIB indicator lights.	*a.* Defective circuit card A5.	*a.* Replace circuit card A5 (para 3–8q and 3–9q).
	b. Defective TRIG SEL DCD MODE SEL switch S27. Isolate by continuity check (fig. FO-19).	*b.* Replace faulty switch S27 (para 3–8f and *3–9b).*
75. Mode 4 reply pulses not present and REPLIES REPLY INHIB indicator lights.	*a.* Defective circuit card A5.	*a.* Replace circuit card A5 (para 3–8q and 3–9q).
	b. Defective circuit card A3.	*b.* (1) Replace circuit card A3 (para 3-8q and *3–9q).* (2) Adjust circuit card A3 (para 3–10c and *d).*
	c. Defective BIT (MOM) switch S37. Isolate by continuity check (fig. FO-19).	*c.* Replace faulty switch S37 (para *3-8f* and *3–9b).*
	d. Defective REPLIES MODULATION SEL switch S20. Isolate by continuity check (fig. FO-19).	*d.* Replace faulty switch S20 (para 3-8f and *3–9b).*
76. No timing markers present.	*a.* Defective circuit card A1.	*a.* (1) Replace circuit card Al (para *3–8q* and *3–9q).* (2) Adjust circuit card Al (para 3-10i).
	b. Defective TIMING MKRS OUT jack J17.	*b.* Replace faulty jack J17 (para *3–8f* and *3–9b).*
77. Improper timing marker levels, spacing or amplitudes.	Defective circuit card A1.	*a.* Replace circuit card Al (para *3–8q* and *3–9q).*
		b. Adjust circuit card Al (para 3–10i).
78. Reply pulses present in external gate input operation.	*a.* Defective circuit card A3.	*a.* (1) Replace circuit card A3 (para *3-8q* and *3–9q).* (2) Adjust circuit card A3 (para 3-10c and *d).*
	b. Defective EXT GATE IN jack J7.	*b.* Replace faulty jack J7 (para *3–8f* and *3–9b).*
79. No MEASUREMENT meter indication in external trigger operation.	Check E trig at TPD7. If normal refer to malfunction 80. If abnormal, fault, is one of the following:	
	a. Defective circuit card A9.	*a.* (1) Replace circuit card A9 (para 3-8q and *3–9q).* (2) Adjust circuit card A9 (para 3–10e (2)(a) through (ac).
	b. Defective TB1,	*b.* Replace TB1 (para *3–8f* and *3–9b).*
	c. Defective TRIG SEL EXT TRIG IN jack J5.	*c.* Replace faulty jack J5 (para *3–8f* and *3–9b).*

Table 3–4. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
80. Normal signal at TPD7.	Check enable trigger at TPB2. If normal refer to malfunction 81. If abnormal, fault is one of the following:	
	a. Defective circuit card A2.	*a.* Replace circuit card A2 (para *3–8q* and 3–9q).
	b. Defective TRIG SEL INT/DCD/EXT switch S24. Isolate by continuity check (fig. FO–19).	*b.* Replace faulty switch S24 (para 3–8f and *3–96).*
81. Normal signal at TPB2.	Defective circuit card A1.	*a.* Replace circuit card Al (para *3–8q* and *3–9q).*
		b. Adjust circuit card Al (para 3–10i).
82. No MEASUREMENT meter movement.	Check signal at M1A1E4. If abnormal, refer to malfunction 83. If normal fault is one of the following	
	a. Defective MEASUREMENT meter M1.	*a.* Replace faulty meter Ml (para 3–8f and *3–9b).*
	b. Defective MEASUREMENT FUNCTION SEL switch S31. Isolate by continuity check (fig. FO–19).	*b.* Replace faulty switch S31 (para 3–8f and *3-9b).*
83. Abnormal signal at M1A1E4.	*a.* Defective amplifier detector AR2.	*a.* Replace faulty AR2 (para 3–8p and 3–9p).
	b. Defective DEMOD VID LEVEL control R4.	*b.* Replace faulty R4 (para *3–8f* and *3–9b).*
84. No pulse train present at DEMOD VID OUT jack.	Check output of SUM RF IN/OUT jack using Square Law Detector RF-210/U. If abnormal refer to malfunction 87. If normal, refer to malfunction 85.	
85. Normal signal at SUM RF IN/OUT jack.	Check signal at DC3J1 using Square Law Detector RF-210/U. If normal, refer to malfunction 86. If abnormal, fault is one of the following	
	a. Defective mult/coupler DC3.	*a.* (1) Replace faulty mult/coupler DC3 (para 3-8j and 3-9j). (2) Adjust rf generator All (para 3–10f).
	b. Defective LOW PWR IN jack J1.	*b.* Replace faulty jack J1 (para *3–8f and 3–9b).*
86. Normal signal at DC3J1.	*a.* Defective circuit card A10.	*a.* (1) Replace circuit card A10 (para *3-8f* and *3-9b).* (2) Adjust circuit card A1O (para 3-10h).
	b. Defective amplifier detector AR2.	*b.* Replace faulty AR2 (para 3–8p and 3–9p).
87. Abnormal signal at SUM RF IN/OUT jack.	Check signal at TPF1 and TPF2 with scope probe. If both are normal refer to malfunction 90. If either is abnormal refer to malfunction 88.	
88. One or both of the signals at TPF1 and TPF2 are abnormal.	Check signal at TPD6 with scope probe. If normal refer to malfunction 89. If abnormal, fault is circuit card A9.	*a.* Replace circuit card A9 (para *3–8f* and *3–9b).* *b.* Adjust circuit card A9 (para 3–10e *(2)(a)* through (ac).

Table 3-4. Troubleshooting Procedure—Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
89. Normal signal at TPD6.	Defective dual modulator A16.	*a.* Replace faulty dual modulator A16 (para 3-8d and 3-9d). *b.* Adjust (para 3–10e).
90. Normal signal at TPF1 and TPF2.	Check signal at A16J2 using Square Law Detector RF-201/U and 15 dB attenuator supplied with test set. Connect 15 dB attenuator to A16J2. If abnormal refer to malfunction 94. If normal refer to malfunction 91.	
91. Normal signal at A16J2.	Check signal at DC2H using Square Law Detector RF-210/U. If normal refer to malfunction 92. If abnormal, fault is coupler DC2.	*a.* Replace faulty coupler DC2 (para 3–8i and *3–9i).* *b.* Adjust (para 3–10e).
92. Normal signal at DC2J1.	Check signal at ATIJ1 using Square Law Detector RF–210/U. If normal refer to malfunction 93. If abnormal, fault is attenuator AT1.	*a.* Replace faulty attenuator AT1 (para *3–8l* and *3–9l).* *b.* Adjust (para 3-10e).
93. Normal signal at ATIJ1.	Defective circulator HY3.	*a.* Replace faulty circulator HY3 (para *3–8n* and *3–9n).* *b.* Adjust (para 3–10e).
94. Abnormal signal at A16J2.	Check signal at HY4J2 using 30 dB attenuator supplied with test set and Rf Power Meter AN/USM–260. Connect 30 dB attenuator to HY4J2. If abnormal refer to malfunction 95. If normal, fault is dual modulator A16.	*a.* Replace faulty dual modulator A16 (para 3-8d and *3-9d).* *b.* Adjust (para 3–10e).
95. Abnormal signal at HY4J2.	Check power at A11J3 using 30 dB attenuator supplied with test set and Rf Power Meter AN/USM–260. Connect 30 dB attenuator to A11J3. If normal refer to malfunction 96. If abnormal, fault is one of the following	
	a. Defective rf generator A11.	*a.* (1) Replace faulty rf generator All (para *3-8b* and 3-9f). (2) Adjust (para 3-10f).
	b. Defective SIG GEN FUNCTION switch S23.	*b.* Replace faulty switch S23 (para 3–8f and *3-9b).*
96. Normal power at A11J3.	*a.* Defective circulator HY4.	*a.* (1) Replace faulty circulator HY4 (para 3–8r and *3–9r).* *(2)* Adjust (para 3-10e).
	b. Defective attenuator AT9.	*b.* (1) Replace faulty attenuator AT1 (para *3–8l* and *3–9l).* (2) Adjust (para 3-10e).
97. Power indication out of tolerance.	Check power at SUM RF IN/OUT jack using AN/UPM–73. If normal refer to malfunction 98. If abnormal, adjust rf generator All.	Adjust rf generator All (para 3–10f).
98. Normal power level at SUM RF IN/OUT jack.	M1A1 out of adjustment,	Adjust M1A1 (para 3–10g).
99. No pulse train present at DEMOD VID OUT jack in DIFF operation.	Check signal at S35J3 using Square Law Detector RF–210/U. If abnormal refer to malfunction 103, If normal refer to malfunction 100.	

Table 3-4. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
100. Normal signal at S35J3.	Check signal at AT5J2 using Square Law Detector RF-210/U. If normal refer to malfunction 101. If abnormal, fault is attenuator AT5.	*a.* Replace faulty attenuator AT5 (para 3–8o and 3–9o). *b.* Adjust (para 3– 10*e).*
101. Normal signal at AT5J2.	Check signal at DC3J7 using Square Law Detector RF–210/U, If normal refer to malfunction 102. If abnormal, fault is coupler DC3.	*a.* Replace faulty coupler DC3 (para 3–8j and 3–9j). *b.* Adjust (para 3– l0 *e).*
102. Normal signal at DC3J7.	Defective attenuator AT4.	*a.* Replace faulty attenuator AT4 (para *3–8m* and *3–9m).* *b.* Adjust (para 3–10 *e).*
103. Abnormal signal at S35J3.	Check signal at AT2J1 using Square Law Detector RF-210/U. If abnormal refer to malfunction 104. If normal, fault is one of the following:	
	a. Defective rf switch S35.	*a.* (1) Replace faulty rf switch S35 (para *3–8k* and *3–9k).* (2) Adjust (para 3–10e).
	b. Defective SIG GEN NORM/INTERLEAVE switch S36.	*b.* Replace faulty switch S36 (para 3–8 *f* and *3–9b).*
104. Abnormal signal at AT2J1.	Check signal at A16J4 using Square Law Detector RF–210/U and 15 dB attenuator supplied with test set. Connect 15 dB attenuator to A16J4. If normal refer to malfunction 105. If abnormal, fault is dual modulator A16.	*a.* Replace faulty dual modulator A16 (para 3–8d and *3–9d).* *b.* Adjust (para 3– l0e).
105. Normal signal A16J4.	Defective attenuator AT2.	*a.* Replace faulty attenuator AT2 (para 3-8 *l* and 3–9 *l).* *b.* Adjust (para 3– 10e).
106. Improper rf power out of DEMOD VID OUT jack in DIFF operation.	Adjust per corrective action. If abnormal refer to malfunction 107.	Adjust (para 3– 10e(2)(an) through *(bf)).*
107. Proper interleave but improper DIFF out.	Defective attenuator AT5.	*a.* Replace faulty attenuator AT5 (para 3–8 *o* and 3–9 *o).* *b.* Adjust (para 3–10 *e* (2)(an) through *(bf)).*
108. Signal present in interleave operation.	*a.* Defective rf switch S35.	*a.* (1) Replace faulty rf switch S35 (para *3–8k* and *3–9k).* (2) Adjust (para 3– 10 *e (2)(an)* through *(bf)).*
	b. Defective SIG GEN NORM/INTERLEAVE switch S36. Isolate by continuity check (fig. FO-19).	*b.* Replace faulty switch S36 (para 3–8.f and *3–9b).*
109. No interleaved pulse trains.	Check signal at TPD5. If normal refer to malfunction 110. If abnormal, fault is one of the following:	
	a. Defective circuit card A9.	*u.* (1) Replace circuit card A9 (para 3-8 *f* and *3–9b).* (2) Adjust (para 3-10e *(2)(a)* through *(ac)).*
	b. Defective SIG GEN NORM/INTERLEAVE switch S36. Isolate by continuity check (fig. FO–19).	b. Replace faulty switch S36 (para 3–8 *f* and 3–9b).

Table 3-4 Troubleshooting Procedure—Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
110. Normal signal at TPD5.	Check signal at S35J1 using Square Law Detector RF-210/U. If normal refer to malfunction 111. If abnormal, fault is one of the following	
	a. Defective SIG GEN NORM/INTERLEAVE switch S36. Isolate by continuity check (fig. FO-19).	***a.*** Replace faulty switch S36 (para 3–8 *f* and *3–9b).*
	b. Defective rf switch S35.	***b.*** (1) Replace faulty switch S35 (para *3-8f* and *3–9b)* (2) Adjust (para 3– l0 *e* (2) *(an)* through *(bf)).*
111. Normal signal at S35J1.	Check signal at S34J2 using Square Law Detector RF–210/U. If normal refer to malfunction 112. If abnormal, fault is one of the following	
	a. Defective SIG GEN NORM/INTERLEAVE switch S36. Isolate by continuity check (fig. FO–19).	***a.*** Replace faulty switch S36 (para *3–8f* and *3–9b).*
	b. Defective rf switch S34.	***b.*** (1) Replace faulty switch S34 (para 3–8 *f* and *3-9 b).* (2) Adjust (para 3–10e (a), *(am)* through *(bf).*
112. Normal signal at S34J2.	Defective circuit card Al0.	***a.*** Replace circuit card Al0 (para *3–8q* and *3–9q).* ***b.*** Adjust circuit card A10 (para 3–10 *h).*
113. Interleave pulse spacing out of tolerance.	Defective circuit card A9.	***a.*** Adjust circuit card A l0 (para 3–l0 *e (2)(y)* through (au)).
		b. (1) Replace circuit card A9 (para *3-8f* and *3–9b).* (2) Adjust circuit card A9 (para 3-10e).
114. No DEMOD VID OUT in external modulation operation.	*a*. Defective dual modulator A16.	a. (1) Replace faulty dual modulator A16 (para 3-8 *d* and 3-9 *d).* (2) Adjust (para 3-10 *e).*
	b. Defective EXT MOD IN jack J2.	***b.*** Replace faulty jack J2 (para *3–8f* and *3–9b).*
115. Improper delay in external modulation operation.	Defective dual modulator A16.	***a.*** Replace faulty dual modulator A16 (para *3–8d* and *3–9d).*
		b. Adjust (para 3- l0 *e).*
116. Improper number of markers present in SWP ±5 MHz.	Check signal at TPB5. If abnormal, refer to malfunction 117. If normal, fault is rf generator A11.	***a.*** Adjust rf generator All (para 3-10 *f).*
		b. (1) Replace rf generator All para *3–8b* and 3–9 *f.* (2) Adjust rf generator All (para 3–l0 *f).*
117. Abnormal signal at TPB5.	Check signal at TPB6. If normal, refer to malfunction 118. If abnormal, fault is one of the following:	
	a. Defective SIG GEN FUNCTION switch S23. Isolate by continuity check (fig. FO–19).	*a.* Replace faulty switch S23 (para *3–8f* and *3–9b).*

Table 3–4. Troubleshooting Procedure -Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
117. (cont.)	*b.* Defective rf generator All.	*b.* (1) Replace rf generator All (para *3-8b* and 3–9 *f).* (2) Adjust rf generator All (para 3–l0 *f).*
118. Normal signal at TPB6.	a. Defective circuit card A3.	*a.* (1) Replace circuit card A3 (para 3-8 *q* and *3–9q).* *(2)* Adjust circuit card A3 (para 3-10 *c* and *d).*
	b. Defective MEASUREMENT FREQ MEAS control R3.	*b* Replace faulty control (para 3-8 *f* and *3–9b).*
119. Improper number of markers present in SWP ±15 MHz	*a.* Defective SIG GEN FUNCTION switch S23. Isolate by continuity check (fig. FO– 19).	*a* Replace faulty switch S23 (para 3-8 *f* and *3–9b).*
	b. Defective rf generator All.	*b.* (1) Replace rf generator All (para *3-8b* and 3–9 *f).* (2) Adjust rf generator All (para 3–l0 *f).*
120. No frequency signal.	Check power at A11J4 using Rf Power Meter AN/USM–260. If normal, refer to malfunction 121. If abnormal, fault is rf generator All.	*a.* Replace rf generator All (para *3–8b* and 3–9 *f).* *b.* Adjust rf generator All (para 3–10 *f).*
121. Normal power at A11J4.	*a,* Defective circuit card A10.	*a.* (1) Replace circuit card A10 (para 3-8q and *3–9q).* *(2)* Adjust circuit card Al0 (para *3-10h).*
	b. Defective rf BIT mixer A15.	*b.* Replace faulty rf BIT mixer A15 (para 3–8 *c* and 3–9 *e).*
	c. Defective amplifier/filter A14.	*c.* Replace faulty amplifier/filter A14 (para 3–8 *e* and 3–9 *c).*
	d. Defective BIT (MOM) switch S37. Isolate by continuity check (fig. FO–19).	*d.* Replace faulty switch S37 (para 3–8 *f* and *3–9b).*
	e. Defective MEASUREMENT FUNCTION SEL switch S31. Isolate by continuity check (fig. FO–19).	*e.* Replace faulty switch S31 (para 3–8 *f* and *3–9b).*

Section III. REMOVAL AND REPLACEMENT

3-8. Removal

All parts may be removed using standard tools and maintenance procedures. Use a 5/16-in. open end wrench to loosen and remove semi-rigid coaxial cables. Refer to figures 3–2 through 3–5 when removing parts and subassemblies.

a. Removal of Test Set Chassis from Dust Cover.

(1) Disconnect all cables from test set.

(2) Loosen 12 captive screws around edge of front panel (four on top, four on bottom, and two on each side).

(3) Pull test set chassis from dust cover.

b. Removal of RF Generator A11.

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3-2 for parts location.

NOTE

To remove connectors P2 and P5, slide retaining clips (part of A11J1 and A11J2) free from locked position. Carefully remove P2 and P5 by slowly rocking and pulling the flange ends of connections. Do not pull by wiring harness when removing connectors.

(2) Slide retaining clip securing connector *P5* to rf generator A11 and remove connector.

(3) Slide retaining clip securing connector P2 to rf generator A11 and remove connector.

(4) Disconnect cable W9P2 from HY4J1 and W9P1 from rf generator A11J3.

(5) Disconnect cable W24P2 from rf generator A11J4.

(6) Remove four screws securing rf generator All to test set chassis.

(7) Remove rf generator All from test set chassis.

c. *Removal of RF/BIT/Mixer Assembly A15.*

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3–3 for parts location.

(2) Disconnect cable W15P2 from rf bit/mixer assembly A15J1.

(3) Disconnect cable W24P1 from rf bit/mixer assembly A15J2.

(4) Disconnect cable W20P2 from rf bit/mixer assembly A15J3.

(5) Remove two screws securing rf bit mixer assembly to test set chassis.

(6) Remove rf bit/mixer assembly far enough from test set chassis to tag and identify all wired connections.

(7) Tag, identify and unsolder all wired connections between rf bit/mixer assembly and test set chassis.

d. Removal of Dual Modulator Assembly A16.

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3–4 for parts location.

(2) Disconnect cable W25P2 from dual modulator A16J1.

(3) Disconnect cable W10P1 from dual modulator A16J2.

(4) Disconnect cable W4P2 from dual modulator A16J4.

(5) Remove four screws securing dual modulator to test set chassis.

(6) Remove dual modulator far enough from test set chassis to tag and identify all connections between dual modulator and test set chassis.

(7) Tag, identify and unsolder connections between dual modulator and test set chassis.

(8) To remove circuit board A16A1, tag, identify and unsolder connections between dual modulator cavity and circuit board.

(9) Remove four screws securing circuit board to top of dual modulator.

(10) If necessary, remove load AT6 from dual modulator A16J3 using a 5/16-in. open end wrench.

e. *Removal of Filter/Amplifier A14.*

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3–4 for parts location.

(2) Disconnect cable W20P1 from filter/amplifier A14J1.

(3) Disconnect cable W22P1 from filter/amplifier A14J2.

(4) Remove four screws securing filter/amplifier A14 to test set chassis.

(5) Remove filter/amplifier far enough from test set chassis to tag and identify connections between filter/amplifier and test set chassis.

(6) Tag, identify and unsolder connections between filter/amplifier and test set chassis.

f. Control Panel Removal for Access.

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3-5 for parts location.

(2) Remove nut and lock washer from LOW PWR IN jack at front of control panel.

(3) Disconnect cable W7P1 from circulator HY3J3.

(4) Disconnect cable W8P1 from attenuator AT4J1.

(5) Disconnect cable W3Pl from DIFF/INTERLEAVE ATTEN control AT2J1.

(6) Disconnect cable W4PI from DIFF/INTERLEAVE ATTEN control AT2J2.

(7) Disconnect cable W2P1 from SUM ATTEN control AT1J2.

(8) Remove eight screws (four on each side) from sides of control panel.

(9) Remove five screws securing control panel to brace behind SUM and DIFF/INTERLEAVE ATTEN controls.

(10) Remove two screws securing front panel to brace next to SIF CHAL VID section of panel.

(11) Remove screw securing HY3 to side of chassis.

(12) Move panel away from test set chassis to clear LOW PWR IN jack HY3 and AT4, then lay panel face down in front of test set chassis.

g. *Power Supply PS1 Removal*

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3-2 for parts location.

(2) From bottom of test set, loosen the two retaining screws and disconnect P1 from power supply PSIJ1.

(3) Remove two screws holding power supply bracket to card cage.

(4) Remove seven screws securing power supply PS1 to rear of test set chassis and three screws securing power supply PS1 to side of test set chassis.

(5) Remove power supply PS1 from the bottom of the test set chassis.

h. Removal of Load AT6, AT7, and AT9.

(1) Remove test set chassis from dust cover *(a,* above) and refer to figures 3–2 and 3–4 for parts location.

(2) Unscrew load from connector.

i. *Removal of Coupler DC2.*

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3– 4 for parts location.

(2) Disconnect cable W10P2 from coupler DC2J3.

(3) Disconnect attenuator ATl0 from coupler DC2J2.

(4) Disconnect cable W2P2 from coupler DC2J1.

(5) Remove two screws securing coupler to test set chassis and remove coupler from test set chassis.

j. Removal of Coupler DC3.

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3– 2 for parts location.

(2) Disconnect cable W18P1 from coupler DC3J1.

(3) Disconnect cable W16P1 from coupler DC3J2.

(4) Disconnect cable W17P1 from coupler DC3J3.

(5) Disconnect cable W19P1 from coupler DC3J4.

(6) Disconnect cable W15P1 from coupler DC3J5.

(7) Disconnect cable W7P2 from coupler DC3J6.

(8) Disconnect cable W8P2 from coupler DC3J7.

(9) Disconnect cable W5P1 from coupler DC3J8.

(10) Remove four screws securing coupler to test set chassis and remove coupler from test set chassis.

k. Removal of Rf Switches S34 and S35.

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3–4 for parts location.

(2) Tag, identify and disconnect all cabling and load (if attached) from rf switch.

(3) Remove two screws securing rf switch mounting bracket to test set chassis.

(4) Remove rf switch far enough from test set chassis to tag and identify all wired connections.

(5) Tag, identify and unsolder all wired connections between rf switch and test set chassis,

(6) Remove rf switch and mounting bracket.

(7) Remove two screws securing rf switch to mounting bracket.

l. Removal of SUM and DIFF/INTERLEAVE ATTEN controls AT1 and AT2.

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3– 5 for parts location.

(2) Tag, identify and disconnect two cables from rear of control.

(3) Remove four screws, flatwashers, lock washers, and nuts securing control to control panel and remove attenuators from front of control panel.

m. Removal of Attenuator AT4.

(1) Remove test set chassis from dust cover (a, above) and refer to figure 3– 5 for parts location.

(2) Unscrew cable W8P1 from rear of attenuator AT4.

(3) Remove protective cap from front of attenuator AT4.

(4) Remove four screws, lock washer, flatwashers, and nuts securing attenuator AT4 to control panel and remove attenuator from control panel.

n. Removal of Circulator HY3.

(1) Remove test set chassis from dust cover (a, above) and refer to figure 3– 5 for parts location.

(2) Disconnect cable WlP2 from circulator HY3J1.

(3) Disconnect cable W7P1 from circulator HY3J3.

(4) Remove protective cap, nut, and washer from circulator HY3J2.

(5) Remove two screws securing circulator HY3 to control panel and remove circulator from control panel.

o. *Removal of Attenuator AT5.*

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3–2 for parts location.

(2) Disconnect cable W14P2 from attenuator AT5J1.

(3) Disconnect cable W19P2 from attenuator AT5J2.

(4) Remove four screws securing attenuator to test set chassis and remove attenuator from test set chassis.

p. Removal of Detector Amplifier AR2.

(1) Remove test set chassis from dust cover (a, above) and refer to figure 3– 2 for parts location.

(2) Disconnect cable W16P2 from detector amplifier AR2J1.

(3) Disconnect cable W17P2 from detector amplifier AR2J2.

(4) Disconnect cable W18P2 from detector amplifier AR2J3.

NOTE

To remove connector P6, slide retaining clip (part of AR2J4) free from locked position. Carefully remove P6 by slowly rocking and pulling the flange ends of the connector. Do not pull by the wiring harness when removing the connector.

(5) Slide retaining clip securing connector P6 to detector amplifier AR2 and remove connector.

(6) Remove four screws securing detector amplifier AR2 to test set chassis.

(7) Remove detector amplifier AR2 from test set chassis.

q. Removal of Circuit Cards Al through A10.

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3–4 for parts location.

(2) Loosen screw to free circuit card retaining bar and remove.

(3) Remove circuit card to be replaced.

r. Removal of Circulator HY4.

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3–2 for parts location.

(2) Disconnect cable W9P2 from circulator HY4J1.

(3) Disconnect cable W25P1 from circulator HY4J2.

(4) Remove four screws securing circulator to test set and remove circulator from test set chassis.

s. *Removal of Attenuator AT10.*

(1) Remove test set chassis from dust cover *(a,* above) and refer to figure 3–4 for parts location.

(2) Disconnect cable W12Pl from attenuator AT1O.

(3) Disconnect attenuator A10 from coupler DC2J2.

3-9. Replacement

All parts may be replaced using standard tools and maintenance procedures. Refer to figures 3–2 through 3–5 when replacing parts and sub-assemblies.

CAUTION

Special care should be used when reinstalling cabling and loads. First start and finger tighten connections by hand, then tighten no more than 1/16 turn further using 5/16-in, wrench.

a. Power Supply PS1 Replacement.

(1) Place power supply in test set chassis from the bottom and replace three screws securing power supply to side of test set chassis, refer to figure 3–2 for part mounting location.

(2) Replace seven screws securing power supply to rear of test set chassis and three screws securing power supply PS1 to side of test set chassis.

(3) Replace two screws securing power supply bracket to card cage.

(4) Connect connector P1 to PSIJ1.

(5) Install test set chassis in dust cover (g, below).

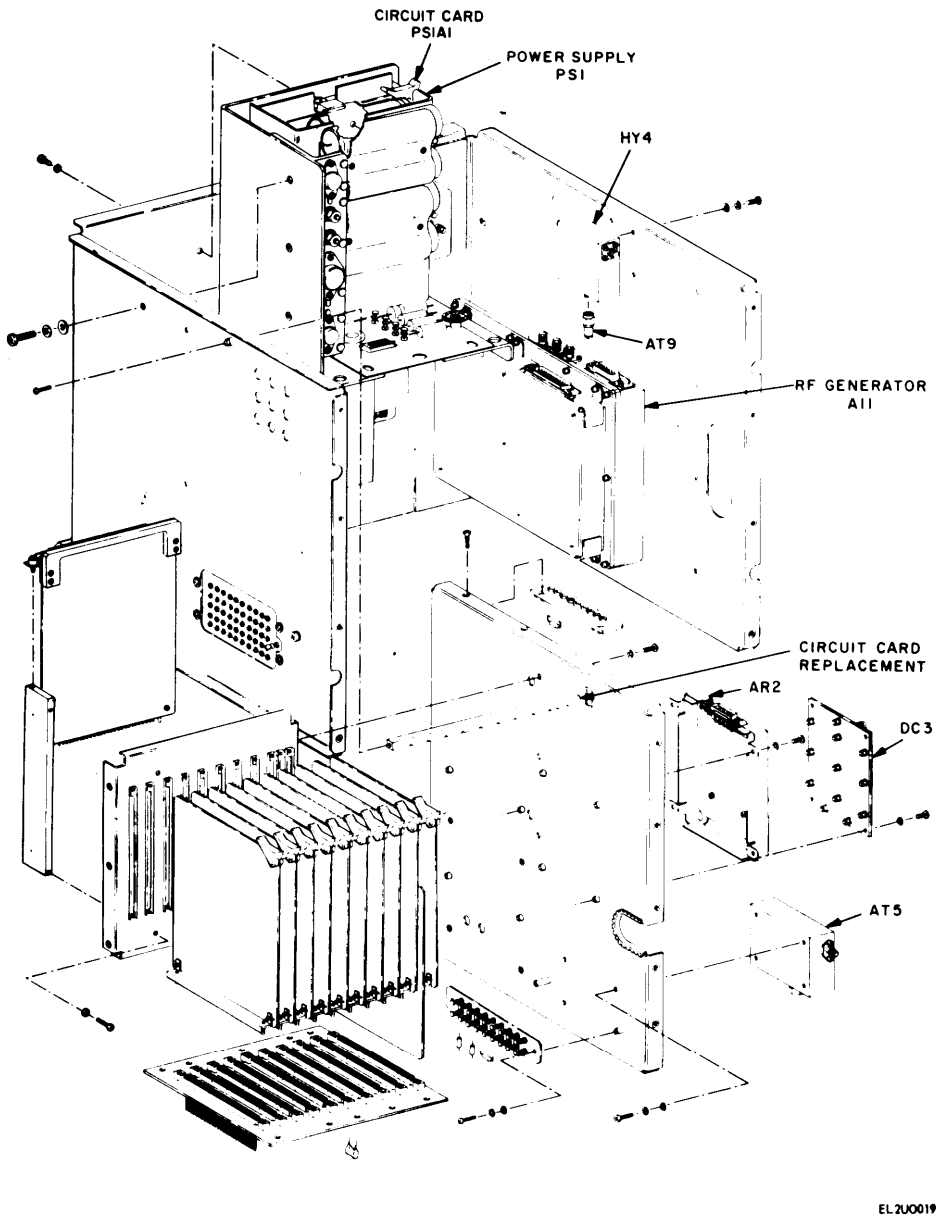


Figure 3-2. Test set chassis (showing main assemblies), partial exploded view.

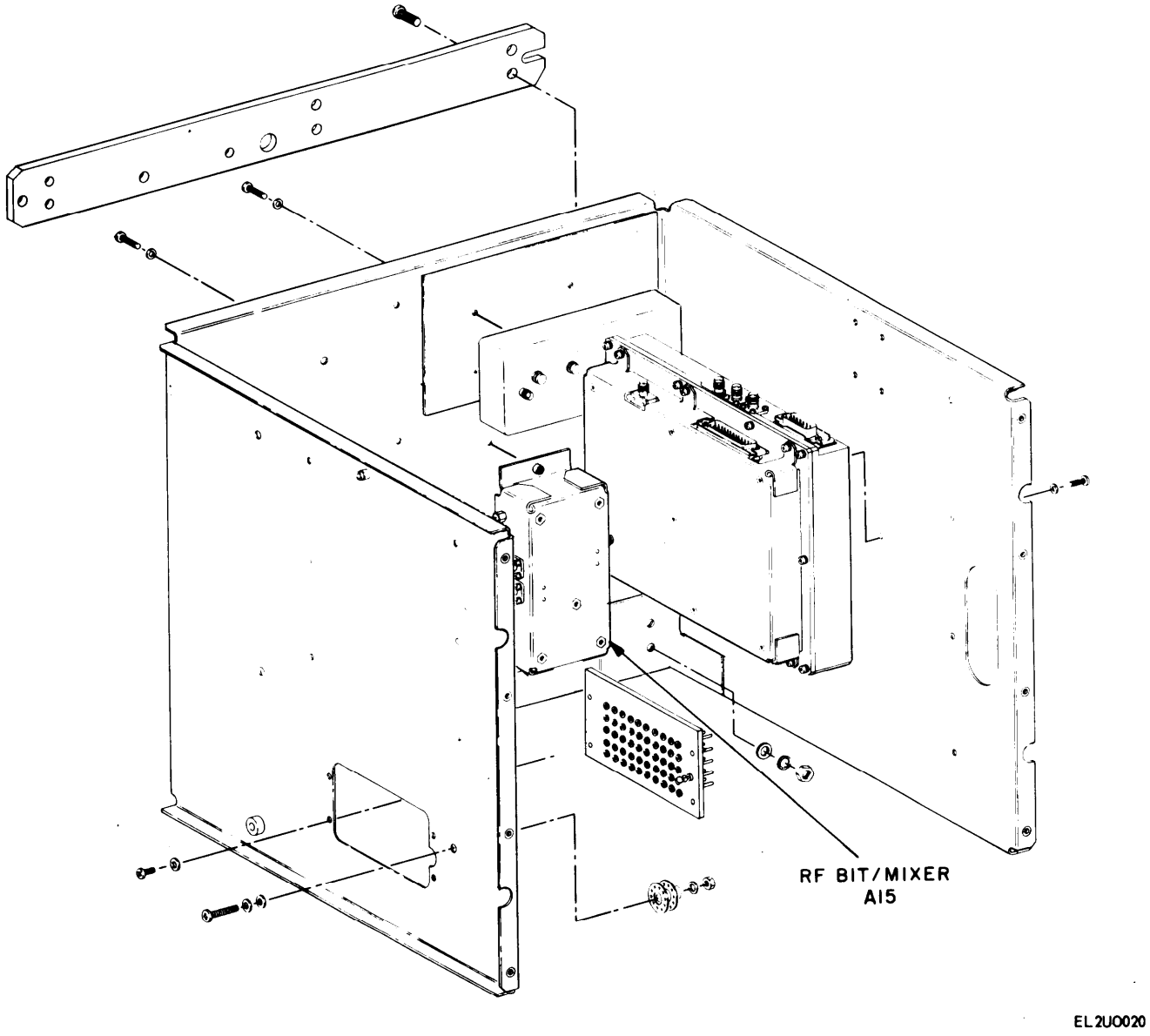


Figure 3–3. *Test set chassis (showing rf bit/mixer A 15), partial exploded view.*

b. Control Panel Replacement.

(1) Refer to figure 3–5 for part mounting location.

(2) Install control panel on front of test set chassis with LOW PWR IN jack projecting through control panel.

(3) Replace two screws which secure brace next to control panel SIF CHAL VID section.

(4) Replace five screws which secure brace next to SUM and DIFF/INTERLEAVE ATTEN controls.

(5) Replace eight screws (four on each side which secure control panel to test set chassis).

(6) Replace nuts and lock washers on LOW PWR IN jack.

CAUTION

First start and tighten connections by hand then tighten no more than 1/16 turn further using 5/16-in. wrench.

(7) Connect cable W2P1 to SUM ATTEN control AT1J2.

(8) Connect cable W3P1 to DIFF/INTERLEAVE ATTEN control AT2J1.

(9) Connect cable W4P1 to DIFF/INTERLEAVE ATTEN control AT2J2.

(10) Connect cable W8P1 to attenuator AT4J1.

(11) Connect cable W7P1 to circulator HY3J3.

(12) Install test set chassis in dust cover (g, below).

c. *Amplifier/Filter A14 Replacement.*

(1) Refer to figure *3–4* for part mounting location.

(2) Connect and solder wiring between amplifier/filter and test set chassis.

(3) Place amplifier/filter in test set and secure with four screws.

CAUTION

First start and tighten connections by hand then tighten no more than 1/16 turn further using 5/16-in. wrench.

(4) Connect connector W22P1 to amplifier/filter A14J2.

(5) Connect cable W20P1 to amplifier/filter A14J1.

(6) Install test set chassis in dust cover (g, below).

d. Dual Modulator A16 Replacement.

(1) Refer to figure 3–4 for part mounting location.

(2) If removed, place circuit board in place on top of dual modulator, secure with four screws and solder wiring between dual modulator and circuit board.

CAUTION

First start and tighten connections finger tight only, then tighten no more than 1/16 turn further, using 5/16-in. wrench.

(3) If removed, replace load AT6 on dual modulator A16J3.

(4) Connect and solder wiring between dual modulator and test set chassis.

(5) Place dual modulator A16 in place in test set chassis and secure in place with four screws.

(6) Connect cable W4P2 to dual modulator A16J4.

(7) Connect cable W10P1 to dual modulator A16J2.

(8) Connect cable W25P2 to dual modulator A16J1.

(9) Install test set chassis in dust cover (g, below).

e. *RF BIT/Mixer Assembly A15 Replacement.*

(1) Refer to figure 3–3 for part mounting location.

(2) Connect and solder wiring between rf bit/mixer assembly A15 and test set chassis.

(3) Place rf bit/mixer assembly A15 in place in test set chassis and secure with two screws.

CAUTION

First start and tighten connections finger tight only, then tighten no more than 1/16 turn further using 5/16-in. wrench.

(4) Connect cable W15P2 to rf bit/mixer assembly A15Jl.

(5) Connect cable W24P1 to rf bit/mixer assembly A15J2.

(6) Connect cable W20P2 to rf bit/mixer assembly A15J3.

(7) Install test set chassis in dust cover *(g*, below).

f. RF Generator A11 Replacement.

(1) Refer to figure 3–2 for part mounting location.

(2) Place rf generator All in place in test set chassis and secure with four screws.

CAUTION

First start and tighten connections finger tight only, then tighten no more than 1/16 turn further using 5/16-in. wrench.

(3) Connect cable W24P2 to rf generator A11J4.

(4) Connect cable W9P1 to rf generator A11J3 and W9P2 to circulator HY4J1.

(5) Connect connector P2 to rf generator A11J1 and secure with retaining clip,

(6) Connect P5 to rf generator A11J2 and secure with retaining clip.

(7) Install test set chassis in dust cover *(g*, below).

g. Test Set Chassis Installation into Dust Cover.

(1) Slide test set chassis into dust cover. Be sure chassis is properly aligned with the guide studs inside dust cover.

(2) Tighten twelve captive screws around edge of test set front panel (four on top, four on bottom and two on each side).

h. Loads AT6, AT7 and AT9 Replacement.

(1) Refer to figures 3–2 and 3–4 for part mounting location.

CAUTION

First start and tighten connections finger tight only, then tighten no more than 1/16 turn further using 5/16-in. wrench.

(2) Screw load onto connector,

(3) Install test set chassis in dust cover (g, above).

i. Coupler DC2 Replacement.

(1) Refer to figure 3–4 for part mounting location.

(2) Attach coupler to test set chassis with two screws.

CAUTION

First start and tighten connections finger tight only, then tighten no more than 1/16 turn further using 5/16-in. wrench.

(3) Connect attenuator ATl0 to coupler DC2J2.
(4) Connect cable W2P2 to coupler DC2J1.
(5) Connect cable W10P2 to coupler DC2J3.
(6) Install test set chassis in dust cover (g, above).

j. Coupler DC3 Replacement.

(1) Refer to figure 3–2 for part mounting location.

(2) Attach coupler to test set chassis using four screws.

CAUTION

First start and finger tighten connections by hand, then tighten no more than l/16 turn further using 5/16-in. wrench.

(3) Connect cable W5Pl to coupler DC3J8.
(4) Connect cable W8P2 to coupler DC3J7.
(5) Connect cable W7P2 to coupler DC3J6.
(6) Connect cable W15Pl to coupler DC3J5.
(7) Connect cable W19Pl to coupler DC3J4.
(8) Connect cable W17Pl to coupler DC3J3.
(9) Connect cable W16Pl to coupler DC3J2.
(10) Connect cable W18Pl to coupler DC3J1.
(11) Install test set chassis in dust cover *(g;* above).

k. RF Switches S34 and S35 Replacement.

(1) Refer to figure 3–4 for part mounting location.

(2) Attach rf switch to mounting bracket using two screws.

(3) Connect and solder wiring between rf switch and test set chassis.

(4) Attach rf switch to test set chassis using two screws.

CAUTION

First start and finger tighten connection by hand, then tighten no more than l/16 turn further using 5/16-in. wrench.

(5) Attach rf cables and load (if attached) to rf switch.

(6) Install test set chassis in dust cover (g, above).

l. SUM and DIFF/INTERLEAVE ATTEN Controls AT1 and AT2 Replacement.

(1) Refer to figure 3–5 for part mounting location.

(2) Insert control through front and attach control panel using four screws, flatwashers, lock washers, and nuts.

CAUTION

First start and finger tighten connection by hand, then tighten no more than l/16 turn further, using 5/16-in, wrench.

(3) Attach two cable sat rear of control.
(4) Install test set chassis in dust cover (g, above).

m. Attenuator AT4 Replacement.

(1) Refer to figure 3–5 for part mounting location.

(2) Attach attenuator to control panel using four screws, lock washers, flatwashers and nuts.

(3) Replace protective cap on front of attenuator AT4.

CAUTION

First start and finger tighten connection by hand, then tighten no more than 1/16 turn further using 5/16-in. wrench.

(4) Attach cable W8P1 to rear of attenuator AT4J1.

(5) Install test set chassis in dust cover (g, above).

n. Circulator HY3 Replacement.

(1) Refer to figure 3–5 for part mounting location.

(2) Attach circulator HY3 to control panel using two screws, nuts, and washers.

(3) Replace protective cap on front of circulator HY3.

CAUTION

First start and finger tighten connections by hand, then tighten no more than 1/16 turn further using 5/16-in. wrench.

(4) Attach cable W7Pl to circulator HY3J3.
(5) Attach cable WlP2 to circulator HY3J1.
(6) Install test set chassis in dust cover (g, above).

o. Attenuator AT5 Replacement.

(1) Refer to figure 3–2 for part mounting location.

(2) Attach attenuator to test set chassis using four screws.

CAUTION

First start and finger tighten connections by hand, then tighten no more than 1/16 turn further using 5/16-in. wrench.

(3) Connect cable W14P2 to attenuator AT5J1.
(4) Connect cable W19P2 to attenuator AT5J2.
(5) Install test set chassis in dust cover (g, above).

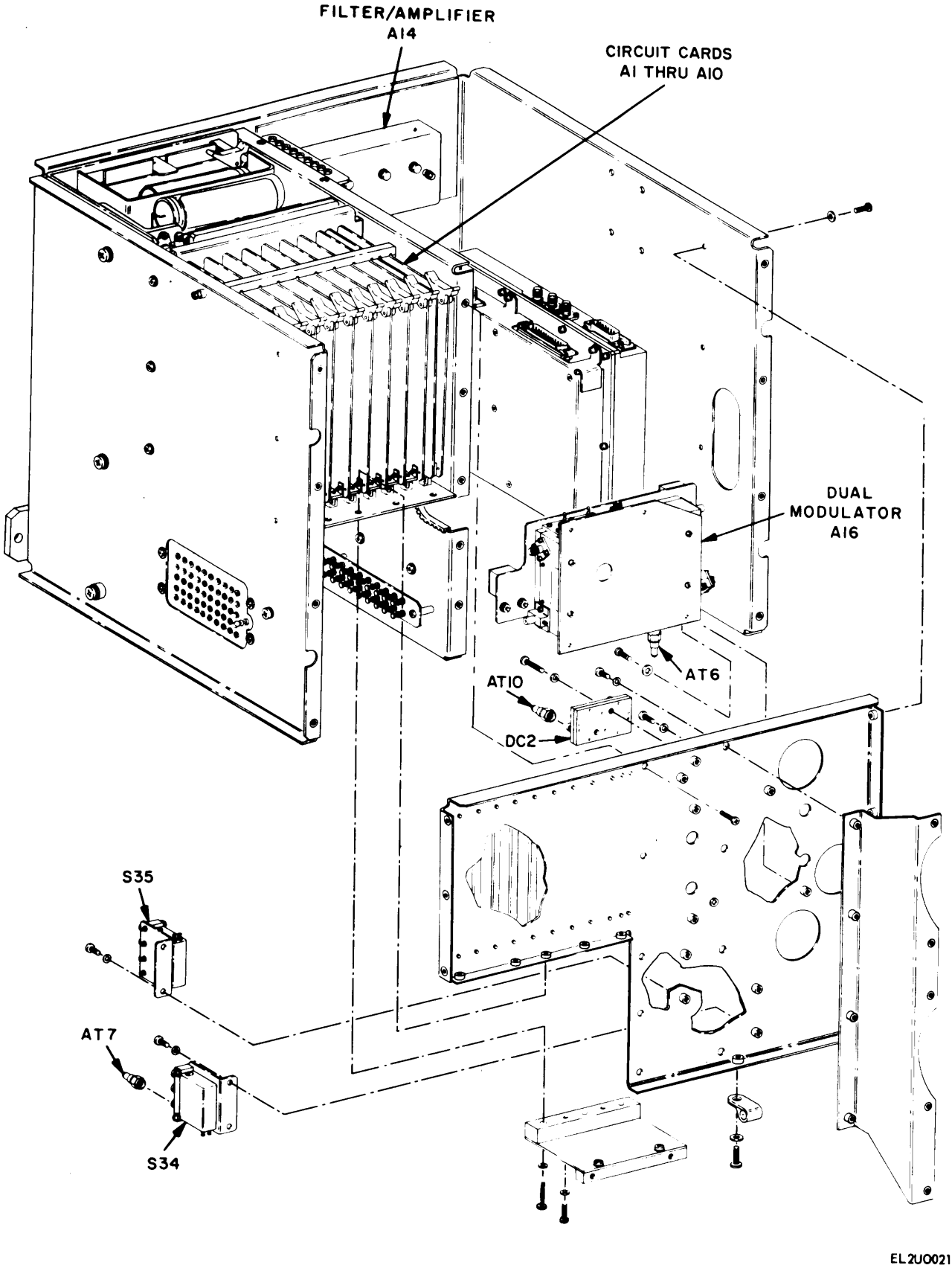


Figure 3-4. Test Set chassis (showing circuit cards), partial exploded view.

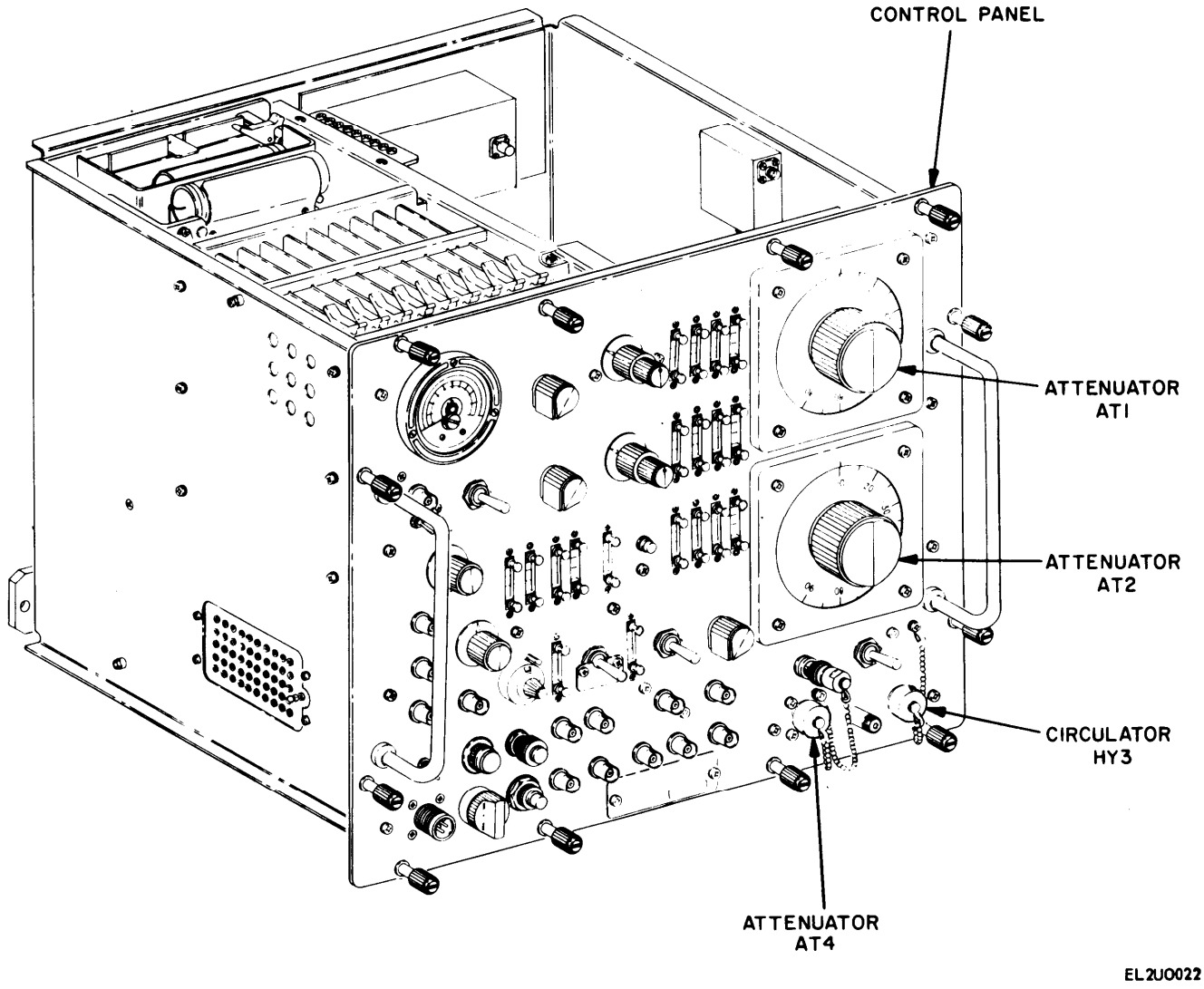


Figure 3-5. Test Set overall view.

p. Detector Amplifier AR2 Replacement.

(1) Refer to figure *3–2* for part mounting location.

(2) Attach attenuator to test set chassis using four screws,

CAUTION

First start and tighten connections by hand, then tighten no more than 1/16 turn further using 5/16-in. wrench.

(3) Connect cable W16P2 to detector amplifier AR2J1.

(4) Connect cable W17P2 to detector amplifier AR2J2.

(5) Connect cable W18P2 to detector amplifier AR2J3.

(6) Secure connector P6withthe slide retaining clip.

(7) Install test set chassis in dust cover (g, above).

q. Circuit Card A1 through A10 Replacement.

(1) Refer to figure 3–4 for part replacement location.

(2) Install replacement circuit card.

(3) Install circuit card retaining bar and secure with screw.

(4) Install test set chassis in dust cover (g, above).

r. Circulator HY4 Replacement.

(1) Refer to figure 3–2 for part mounting location.

(2) Attach circulator to test set chassis using four screws.

CAUTION

First start and tighten connections by hand, then tighten no more than 1/16 turn further using 5/16-in. wrench.

(3) Connect cable W25Pl to circulator HY4J2.
(4) Connect cable W9P2 to circulator HY4J1.
(5) Install test set chassis in dust cover *(g,* above).

s. *Attenuator AT10 Replacement.*

(1) Refer to figure 3–4 for part mounting location.

CAUTION

First start and tighten connections by hand, then tighten no more than 1/16 turn further using 5/16-in. wrench.

(2) Connect attenuator AT10 to coupler DC2J2.
(3) Connect cable W12Pl to attenuator AT10.
(4) Install test set chassis in dust cover (g, above).

Section IV. ADJUSTMENT AND ALIGNMENT

3–10. Adjustment Procedures

a. Initial Procedures

(1) Test point locations are shown in figure 3–1, and adjustment locations are shown in figure 3–6.
(2) Perform the starting procedures as outlined in paragraph 3–4.

(3) Remove power from the test set when removing or replacing circuit boards or the extender board.

b. Power Supply Adjustment

(1) Test equipment required.
(a) Transformer CN–16A/U, variable
(b) Multimeter ME–26B/U

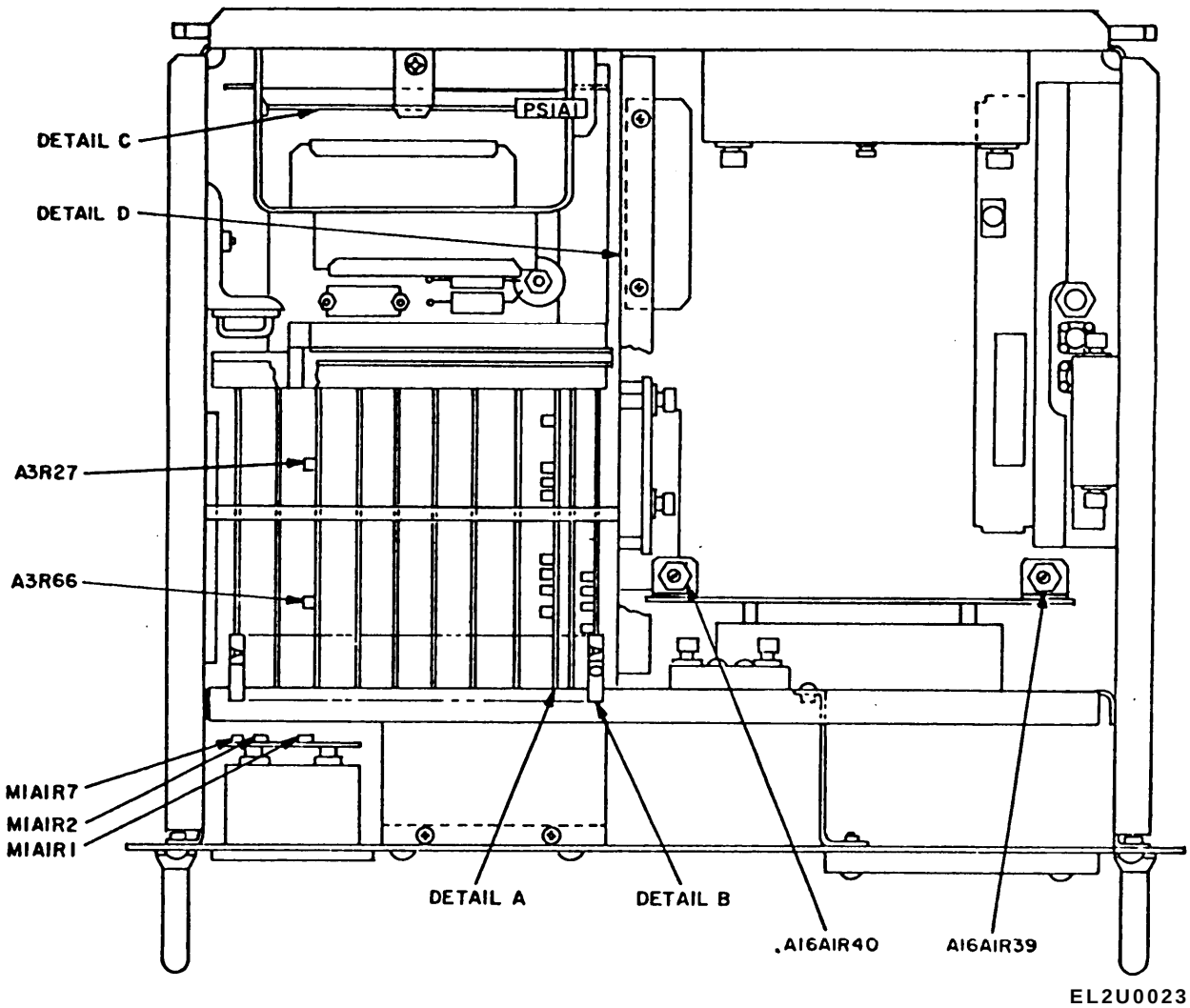


Figure 3– 6. Adjustment location diagram (sheet 1 of 2).

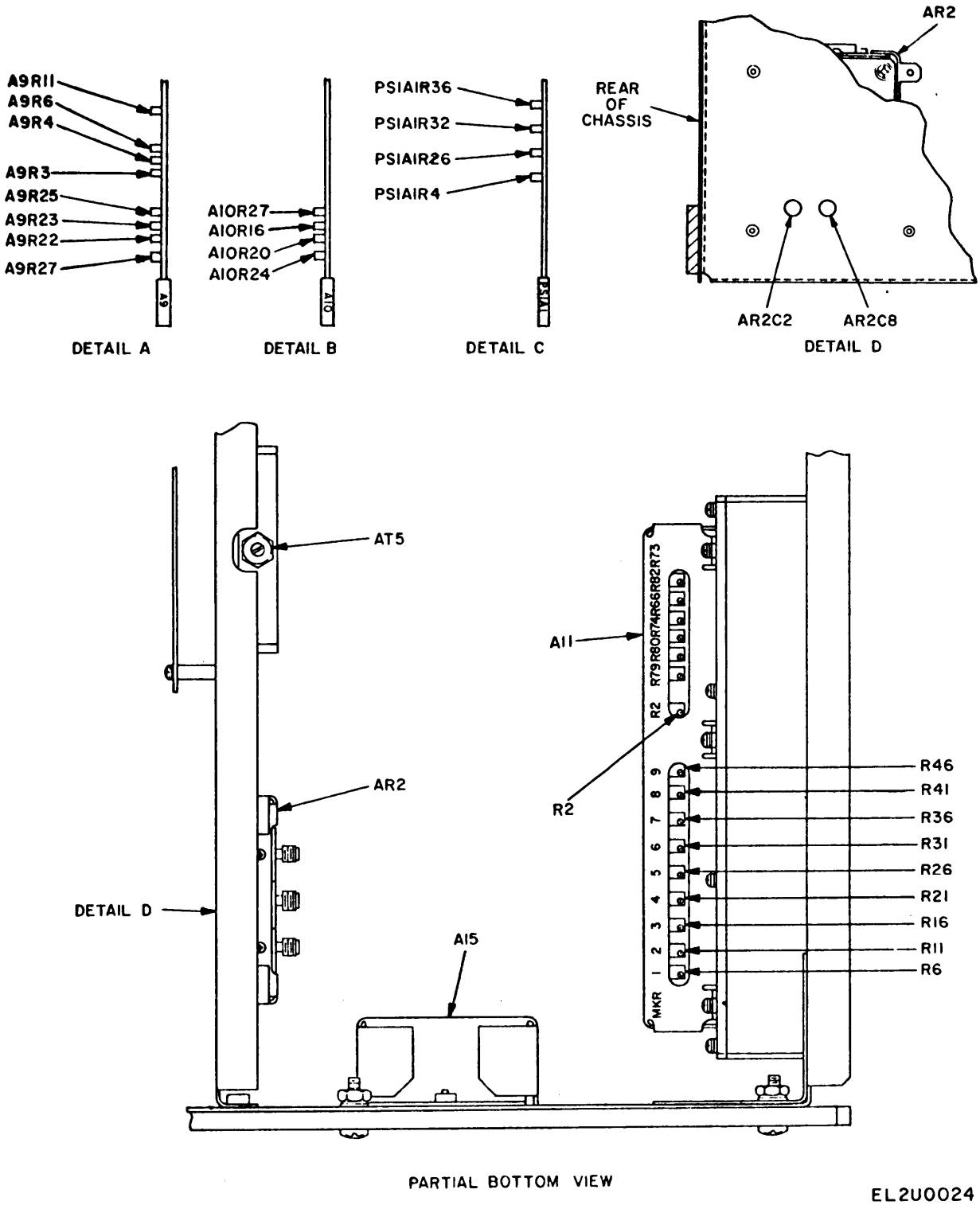


Figure 3-6. Adjustment location diagram (sheet 2 of 2).

(c) Differential Voltmeter ME–202B/U

(2) Adjustment Procedure

NOTE

Operate differential voltmeter in accordance with procedures in TM 11–6625–537–15.

(a) Connect test setup as shown in figure 3–7.

(b) Adjust transformer until multimeter indicates 115vac.

(c) Set test set controls as listed in table 3–1.

(d) Set differential voltmeter NULL switch to VTVM.

(e) Connect differential voltmeter (+) probe of PS1A1TP1 and (-) probe to GND.

(f) Adjust PS1A1R4 until differential voltmeter indicates 28.00 volts (+ voltage).

(g) Connect differential voltmeter (+) probe to PS1A1TP5.

(h) Adjust PS1A1R26 until differential voltmeter indicates 12.00 volts (+ voltage).

(i) Connect differential voltmeter (+) probe to PS1A1TP7.

(j) Adjust PS1A1R36 until differential voltmeter indicates 5.00 volts (+ voltage).

(k) Connect differential voltmeter (-) probe to PSlAlTP6 and (+) probe to GND.

(l) Adjust PS1A1R32 until differential voltmeter indicates 12.00 volts (- voltage).

(m) Check operation of DC FAULT indicator circuit by adjusting power supply outputs as listed in table 3–5. If improper DC FAULT indicator status is noted, power supply PSI is faulty and should be replaced.

c. *Mode 4 Challenge Video Pulse Width Adjustment.*

(1) *Test equipment required.*

Oscilloscope AN/USM–281A

(2) *Adjustment procedure*. Perform table 3–28, steps 1 and 2 except do not connect frequency counter, Adjust A3R27 for pulse width of 0.5 ±0.05 µsec at 50 percent of amplitude.

d. SIF Challenge Video Pulse Width Adjustment.

(1) *Test equipment required.*

oscilloscope AN/USM–281A

(2) *Adjustment procedure*. Perform table 3–20, steps 1 through 3 except do not connect frequency counter and adjust A3R66 for pulse width of 0.8 ±0.05 µsec at 50 percent of amplitude for both steps 2 and 3.

e. *Reply Pulse and Rf Power Output Adjustment.*

(1) *Test equipment required.*

(a) Oscilloscope AN/USM–281A

(b) Square Law Detector RF-210/U

(c) Pulse Power Calibrator Set AN/UPM–73

(d) 3-volt DC source

(2) Adjustment procedures.

(a) Connect test setup as shown in figure 3-8.

(b) Set test set controls as listed in table 3-1 except as follows:

Control	*Position*
SUM ATTEN	-10 DB
REPLIES REPLY WIDTH SELECT	0.15
REPLIES MODULATION SEL	M4–lP
POWER	OFF

Table 3–5. DC FAULT Indicator Circuit Check Procedure

Step	Output under test	Differential voltmeter connections		Adjustment	Differential voltmeter indication	DC FAULT indicator status
		(+) Probe	(-) Probe			
1	-12V	GND	PS1A1TP6	PS1A1R32	12.20 vdc (-)	Off
2	-12V	GND	PS1A1TP6	PS1A1R32	13.10 vdc (-)	On
3	-12V	GND	PS1A1TP6	PS1A1R32	11.80 vdc(-)	Off
4	-12V	GND	PS1A1TP6	PS1A1R32	10.90 vdc (-)	On
5	-12V	GND	PS1A1TP6	PS1A1R32	12.00 vdc (-)	Off
6	+28V	PS1A1TP1	GND	PS1A1R4	28.20 vdc (+)	Off
7	+28V	PS1A1TP1	GND	PS1A1R4	29.10 vdc (+)	On
8	+28V	PS1A1TP1	GND	PS1A1R4	27.80 vdc (+)	Off
9	+28V	PS1A1TP1	GND	PS1A1R4	26.90 vdc (+)	On
10	+28V	PS1A1TP1	GND	PS1A1R4	28.00 vdc (+)	Off
11	+12V	PS1A1TP5	GND	PS1A1R26	12.20 vdc (+)	Off
12	+12V	PS1A1TP5	GND	PS1A1R26	13.10 vdc (+)	On
13	+12V	PS1A1TP5	GND	PS1A1R26	11.80 vdc(+)	Off
14	+12V	PS1A1TP5	GND	PS1A1R26	10,90 vdc (+)	On
15	+12V	PS1A1TP5	GND	PS1A1R26	12.00 vdc (+)	Off
16	+5V	PS1A1TP7	GND	PS1A1R36	5.20 vdc (+)	Off
17	+5V	PS1A1TP7	GND	PS1A1R36	4.80 vdc (+)	Off
18	+5V	PS1A1TP7	GND	PS1A1R36	3.90 vdc (+)	On
19	+5V	PS1A1TP7	GND	PS1A1R36	5.00 vdc (+)	Off

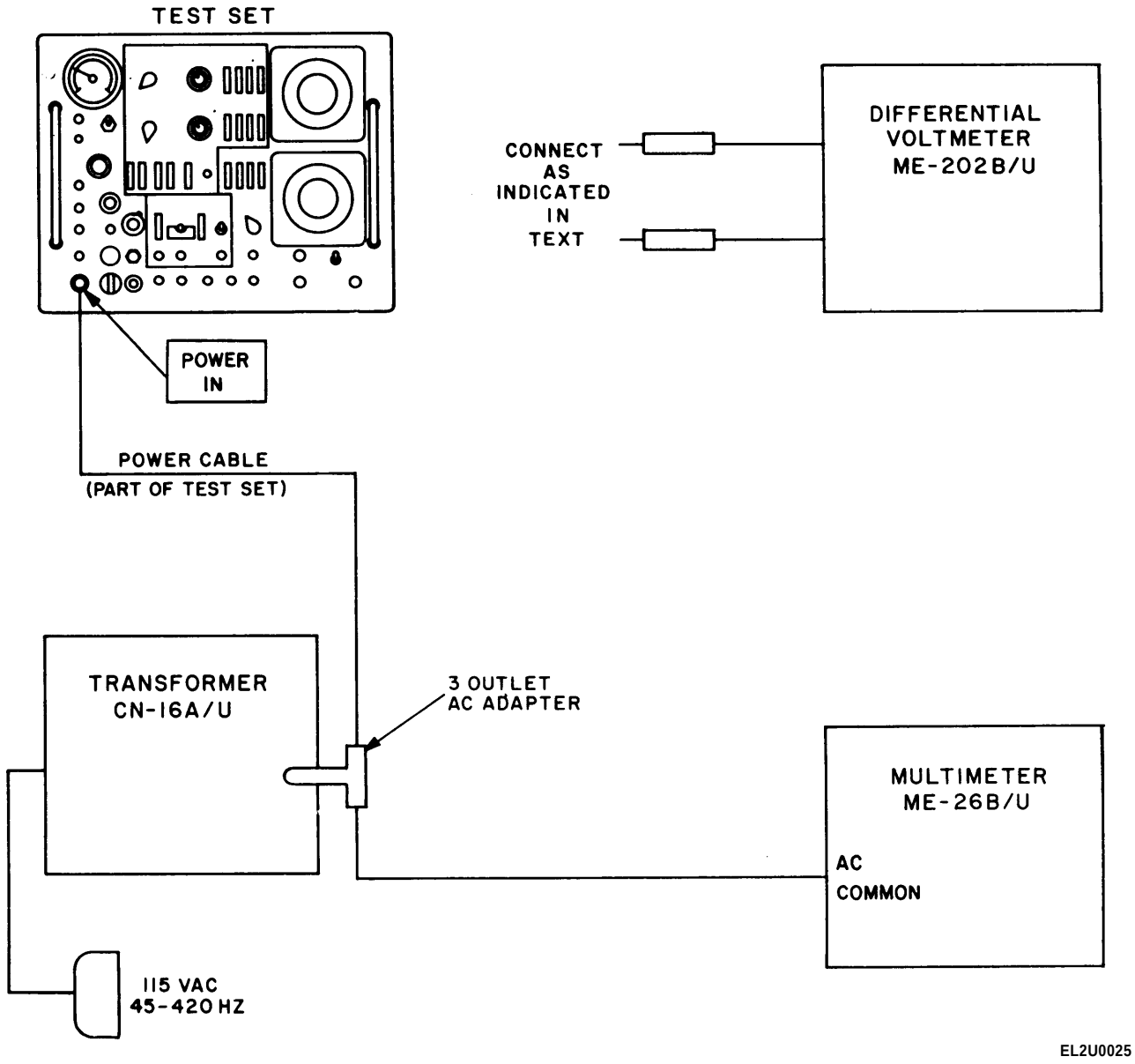


Figure 3-7. Power supply adjustment setup.

(c) Setup oscilloscope (para3–4c).

(d) Remove circuit card shield between circuit cards A9 and Al0.

(e) Remove circuit card A9 and reconnect to test set with extender card (normally stored in slot between card cage and power supply PS1). Set POWER switch to ON.

NOTE

If circuit card A9 has been replaced, perform steps *(a)* through *(ac).* If rf components have been replaced, perform steps *(a), (b),* and *(y)* through *(bf).*

(f) Adjust A9R3 until pulse is 0.15 µsec wide at 50% of pulse amplitude.

(g) Set REPLIES REPLY WIDTH SELECT switch to 0.45.

(h) Adjust A9R4 until pulse is 0.45 µsec wide at 50% of pulse amplitude.

(i) Set REPLIES REPLY WIDTH SELECT switch to 0.50.

(j) Adjust A9R6 until pulse is 0.50 µsec wide at 50% of pulse amplitude.

(k) Set REPLIES REPLY WIDTH SELECT switch to 0.90.

(l) Adjust A9R11 until pulse is 0.90 µsec wide at 50% of pulse amplitude.

(m) Set REPLIES REPLY WIDTH SELECT switch to VARY. Verify pulse varies from less than 0.15 µsec to greater than 1.50 µsec with REPLIES REPLY WIDTH VARY control.

(n) Set test set REPLIES SUB PULSE SEL switch to M4–P3 and REPLIES SUB PULSE POS SELECT switch to VARY.

(o) Adjust oscilloscope to observe pulse.

(p) Repeat step *(m).*

(q) Set REPLIES REPLY WIDTH SELECT switch to 0.90.

(r) Adjust A9R27 until pulse is 0.90 µsec wide at 50% of pulse amplitude.

(s) Set REPLIES REPLY WIDTH SELECT switch to 0.50.

(t) Adjust A9R25 until pulse is 0.50 µsec wide at 50% of pulse amplitude.

(u) Set REPLIES REPLY WIDTH SELECT switch to 0.45.

(v) Adjust A9R23 until pulse is 0.45 µsec wide at 50% of pulse amplitude.

(w) Set REPLIES REPLY WIDTH SELECT switch to 0.15.

(x) Adjust A9R22 until pulse is 0.15 µsec wide at 50% of pulse amplitude.

(v) Set test set controls as follows:

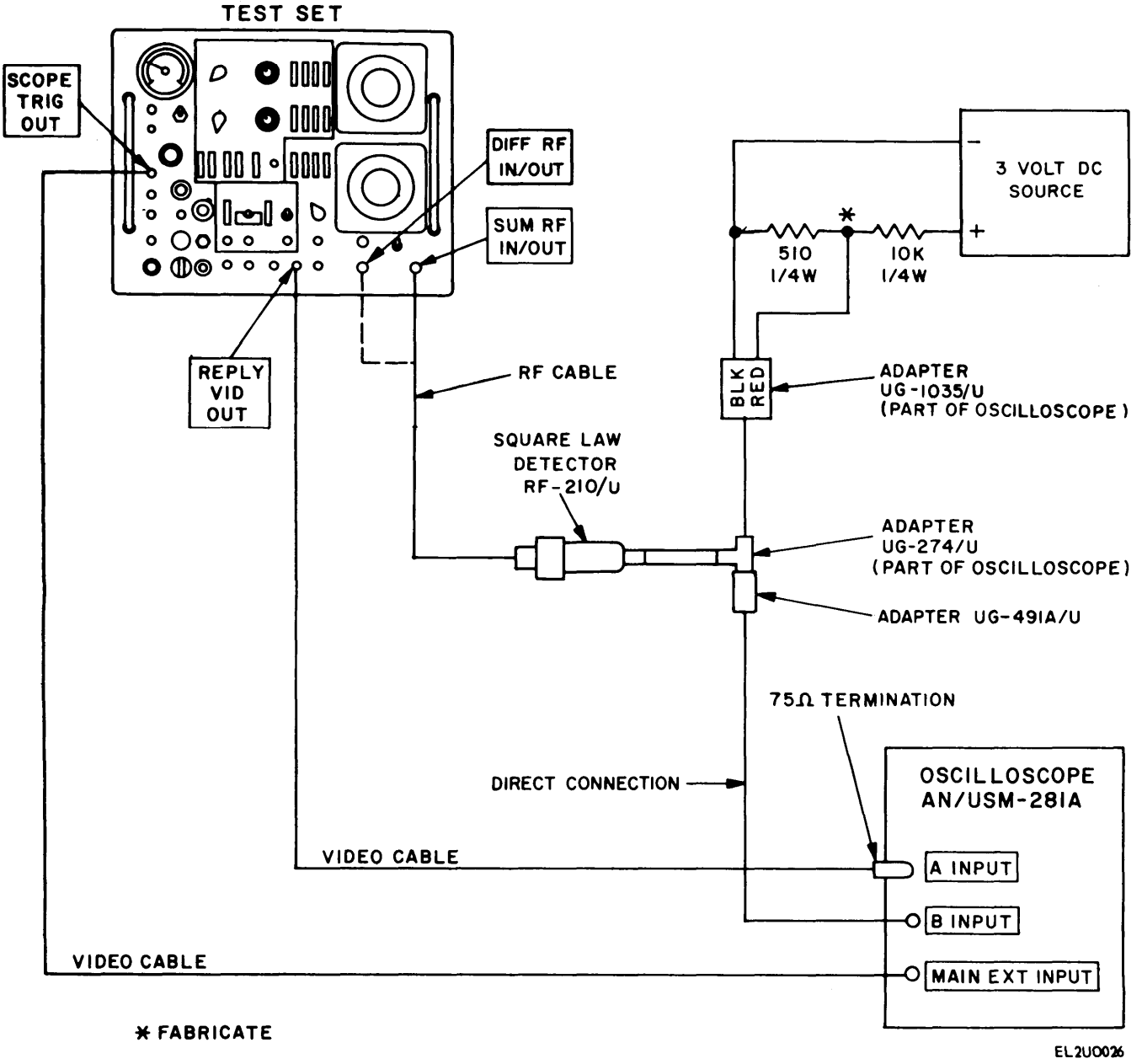


Figure 3-8. Reply pulse width adjustment setup.

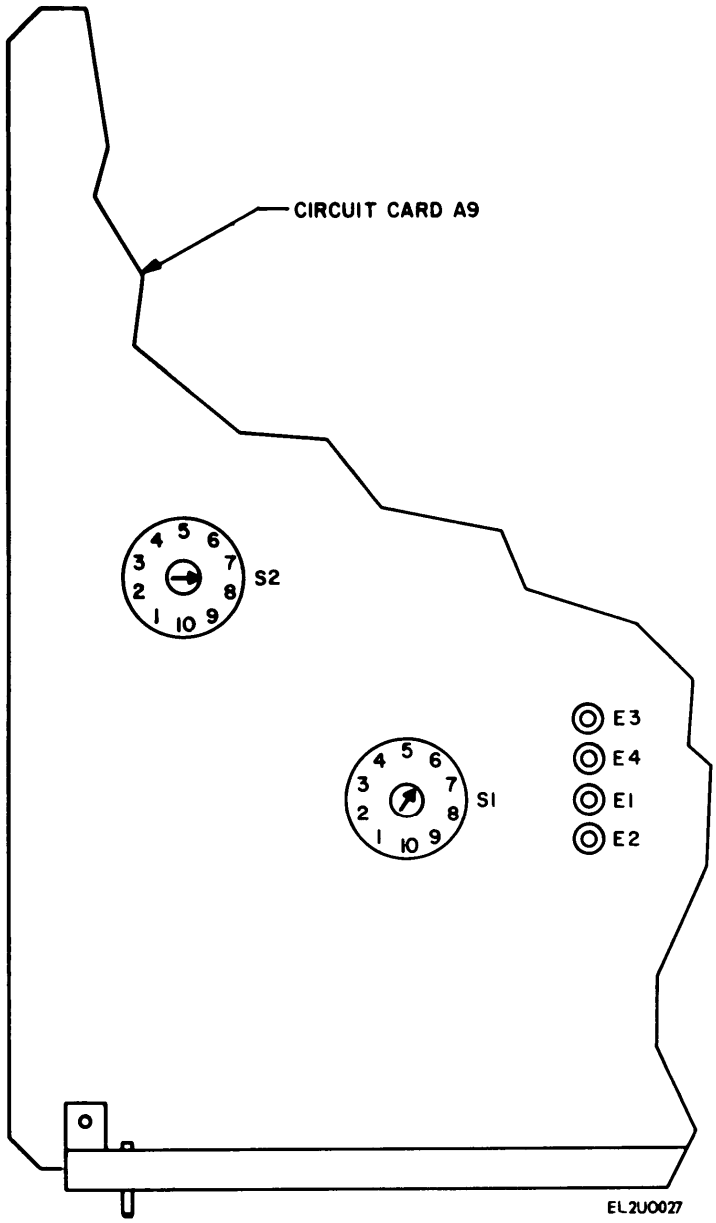


Figure 3–9. Circuit card A9 switch location diagram.

Control	*Position*
REPLIES REPLY WIDTH SELECT	0.50
REPLIES SUB PULSE SEL	OFF
REPLIES SUB PULSE POS SELECT	0
SIG GEN NORM/INTERLEAVE	INTER-LEAVE

(z) Set oscilloscope display switch to B and observe detected sum RF IN/OUT signal at oscilloscope B INPUT.

(aa) Adjust A9S2 for 0.70 ±0.05 µsec spacing between first and second pulse at 50% point of leading edge of pulses. (See figure 3–9 for switch location).

(ab) Adjust A9S1 for 0.50 ±0.05 µsec pulse width of pulse at 50% amplitude.

(ac) Set test set SIG GEN NORM/INTERLEAVE switch to NORM.

(ad) Observe pulse on oscilloscope B INPUT.

(ae) Measure pulse rise and fall times between the 1% and 81% amplitude points. Pulse rise time should be 0.05 to 0.1 µsec and pulse fall time should be 0.05 to 0.2 µsec as shown in A, figure 3–15.

(af) Measure pulse width. Pulse width should be 0.50 ±0.05 ±sec.

NOTE

Perform step *(ag)* if pulse rise time and/or fall time are not in tolerance. Perform steps *(ah)* through *(ak)* if rise time and fall time are in tolerance but pulse width is out of tolerance. Proceed to step *(al)* if rise time, fall time, and pulse width are in tolerance.

(ag) Adjust A16A1R40 until pulse rise time, fall time are in tolerance.

(ah) Remove circuit card A9.

(ai) Remove circuit card shield between circuit cards A9 and Al0.

(aj) Connect extender card and circuit card A9 to test set.

(ak) Adjust A9S1 for 0.50 ±0.05 µsec pulse width at 50% amplitude point.

(al) Perform table 3–30, steps 1 through 5 to determine peak pulse and cw power.

NOTE

If peak power and cw power (table 3–30, steps 3, 4 and 5) are in tolerance proceed to step *(an)*. If peak pulse or cw power is out of tolerance proceed to step *(am)*.

(am) Repeat steps 1 through 4, table 3–30 while adjusting A11A1R2 until cw and pulse power outputs are in tolerance.

(an) Connect test setup as shown in figure 3–8.

(ao) Set test set SIG GEN NORM/INTERLEAVE switch to INTERLEAVE, SUM ATTEN control to -10 DB and REPLIES MODULATION SEL switch to M4–lP.

(ap) Adjust DIFF/INTERLEAVE ATTEN control until second pulse amplitude is equal to first pulse (within ±1 dB).

(aq) Slip DIFF/INTERLEAVE ATTEN control dial plate until 0 mark lines up with indicator mark while maintaining step *(up)*.

NOTE

To slip DIFF/INTERLEAVE ATTEN control dial plate loosen 2 set screws on knob and remove knob. Loosen 4 screws to dial plate and rotate dial plate to desired setting. Reverse sequence to complete reassembly.

(ar) Set test set SIG GEN NORM/INTERLEAVE switch to NORM and DIFF/INTERLEAVE ATTEN control to -10 DB.

(as) Disconnect square law detector from test set SUM RF IN/OUT jack and connect to DIFF RF IN/OUT jack.

(at) Measure pulse rise and fall times between the 1% and 81% amplitude points. Pulse rise time should be 0.05 to 0.1 µsec and pulse fall time should be 0.05 to 0.2 µsec.

(au) Measure pulse width. Pulse width should be 0.50 +0.05 µsec.

NOTE

Perform step *(av)* if pulse rise time, fall time and/or pulse width are not in tolerance. Perform steps *(aw)* through *(ba)* if rise time and fall time are in tolerance but pulse width is out of tolerance. Proceed to step *(bb)* if rise time, fall time and pulse width are in tolerance.

(av) Adjust A16A1R39 until rise time, fall time and pulse width are in tolerance.

(aw) Repeat steps *(ah)* through *(ak)*.

(ax) Disconnect square law detector from test set DIFF RF IN/OUT jack and connect to test set SUM RF IN/OUT jack.

(ay) Verify pulse width is 0.50 +0.05 µsec.

NOTE

Perform step *(az)* and *(ba)* if step *(ay)* is out of tolerance.

(az) Set test set SIG GEN NORM/INTERLEAVE switch to INTERLEAVE.

(ba) Adjust A9S1 until both pulses are within tolerance.

(bb) Set test set SIG GEN NORM/INTERLEAVE switch to NORM, REPLIES MODULATION SEL switch to M4-3P, and DIFF/INTERLEAVE ATTEN control to 0 DB.

(bc) Set equipment as in figure 3–37 except connect cable from rf power meter to DIFF RF IN/OUT jack.

(bd) Perform table 3–30, steps 6 through 10 to determine peak pulse and cw power.

NOTE

Proceed to step *(be)* if peak pulse or cw power is out of tolerance.

(be) Repeat step 5, table 3–30 while adjusting AT5.

(bf) Repeat steps 6, 7, and 8, table 3-30.

f. RF Generator All Adjustment

(1) *Test equipment required.*

(a) Oscilloscope AN/USM-281A

(b) Frequency Comparator CM-77A/USM

(c) Frequency Counter AN/USM-207A

(d) RF Power Meter AN/USM–260

(e) Square Law Detector RF–210/U

(2) *Adjustment procedure.*

(a) Connect test setup as shown in figure 3–l0.

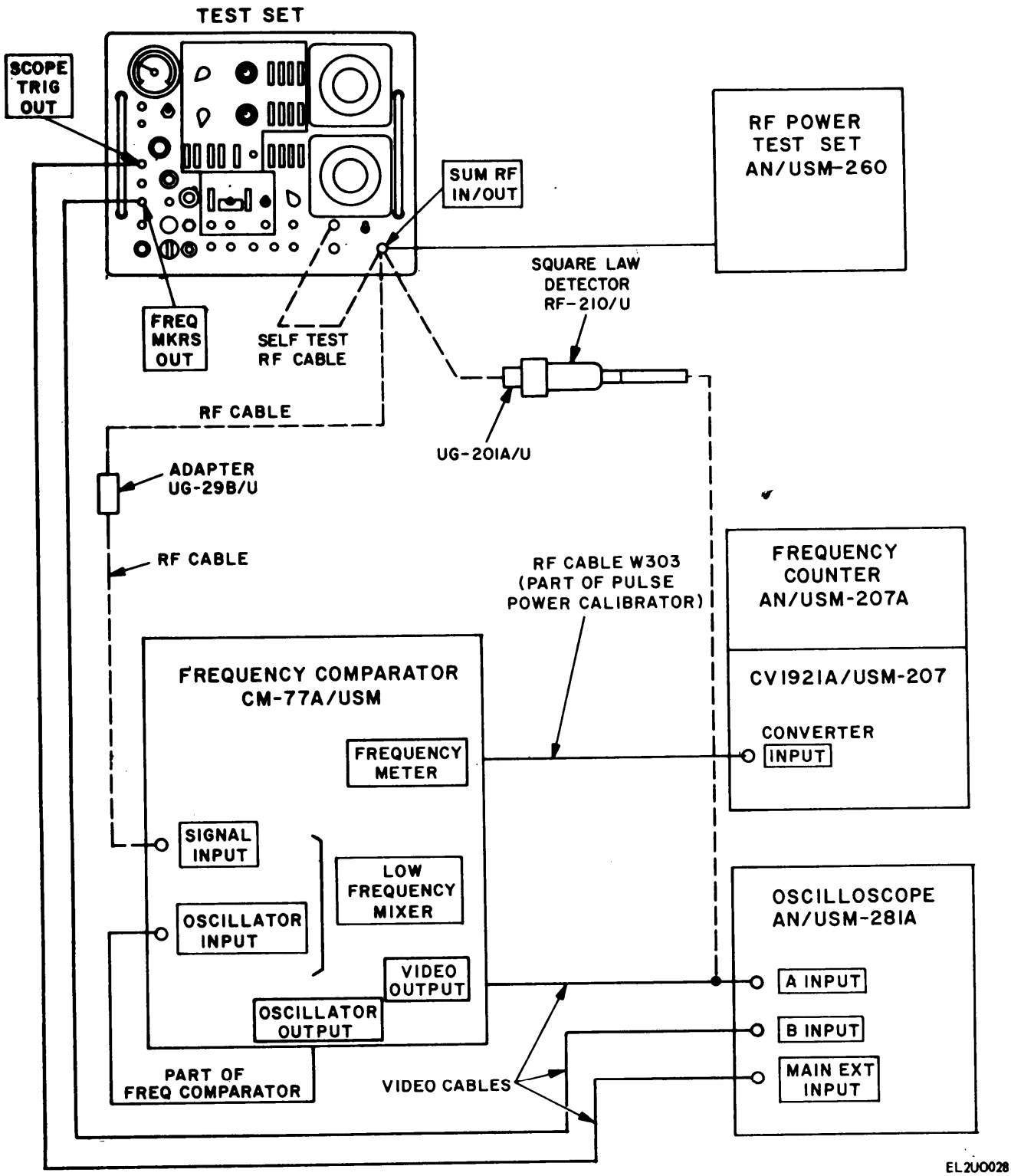


Figure 3-10. RF generator adjustment setup.

(b) Set up oscilloscope, paragraph 3–4c, except set DISPLAY switch to ALT.

(c) Set test set controls as in table 3–1 except set REPLIES MODULATION SEL switch to CW.

(d) Adjust A11A1R2 for 0 dB on rf power meter.

(e) Remove rf power meter from test set SUM RF IN/OUT jack.

(f) Connect frequency comparator signal input to test set SUM RF IN/OUT jack,

(g) Set up frequency counter, paragraph 3–4e, except set the controls as follows:

Control	*Setting*
SENSITIVITY	PLUG IN
FUNCTION	FREQ
DISPLAY	As required
POWER	STORE
FREQUENCY TUNING MC	200
INPUT (two switches)	10V MAX and 10V MAX
DIRECT/HETRODYNE	HETRODYNE
Time base	1

(h) Setup frequency comparator, paragraph 3–4 *f* and set FREQUENCY MEGACYCLES controls to approximately 218 MHz.

NOTE

The frequency comparator is used to zero beat the test set output with the 5th harmonic of the frequency comparator fundamental frequency. The fundamental frequency of frequency comparator is then measured by the frequency counter. During the following steps measure frequency using the following formula: f= (200 MHz + counter reading in MHz) x 5.

(i) To check rf frequency when test set is set for fixed frequency operation, adjust frequency comparator FREQUENCY MEGACYCLES controls until a zero beat is observed on oscilloscope. Calculate frequency. Frequency should be 1090.0 ±0.109 mHz.

(j) Set test set SIG GEN FUNCTION switch to SWP ±15 MHz.

(k) Adjust oscilloscope controls as necessary to view nine makers (B input) and zero beat (A input). Nine markers represent -15, -10, -5, -1, 0, +1, +5, +10 and +15 MHz from 1090 MHz. Zero beat should be at 0 MHz marker.

(l) To check beginning of sweep, adjust frequency comparator VIDEO RESPONSE LOW FREQ control for most defined zero beat. Then adjust FREQUENCY MEGACYCLES controls until zero beat just disappears then reappears at start of sweep, Calculate rf frequency. Frequency at start of sweep should be 1070.0 MHz ±0.5 MHz.

(m) To check end of sweep, adjust frequency comparator FREQUENCY MEGACYCLES controls until zero beat just disappears then reappears at end of sweep. Calculate rf frequency. Frequency at end of sweep should be 1108 MHz ±0.5 MHz.

(n) Adjust frequency comparator FREQUENCY MEGACYCLES controls to align zero beat with leading edge of each marker. Frequency of each marker should be as indicated below:

NOTE

Use oscilloscope delay function as necessary to accurately observe alignment.

Marker	Adjust	*Frequency*
1 (-15 MHz)	A11A1R6	1075.0 ±0.3 MHz
2 (-10 MHz)	A1lAIR1l	1080.0 ±0.3 MHz
3 (-5 MHz)	A11A1R16	1085.0 ±.1 MHz
4 (-1 MHz)	A11A1R21	1089.0 ±0.1 MHz
5 (0 MHz)	A11A1R26	1090.0 ±0.1 MHz
6 (+ l MHz)	A11A1R31	1091.0 ±0.1 MHz
7 (+5 MHz)	A11A1R36	1095.0 ±0.1 MHz
8 (+10 MHz)	A11A1R41	1100.0 ±0.3 MHz
9 (+15 MHz)	A11A1R46	1105.0 ±0.3 MHz

(o) Set test set SIG GEN FUNCTION sweep to SWP ±5 MHZ. Observe five frequency markers (B input), representing -5, -1, 0, +1, +5 MHZ.

(p) Set test set SIG GEN FUNCTION switch to SWP ±15 MHZ, SUM ATTEN control to -5 DB and REPLIES MODULATION SEL switch to 30 KHZ.

(q) Remove rf cable from test set SUM RF IN/OUT jack.

(r) Connect square law detector to test set SUM RF IN/OUT jack and connect oscilloscope A INPUT to square law detector output using video cable.

(s) Adjust oscilloscope A VOLTS/DIV switch and A POSITION control as necessary to view 30 KHz pulses.

NOTE

During following steps, high and low amplitude negative pulses are to be located *between +15* and -15 MHz markers.

(t) Observe negative pulse with greatest amplitude (high pulse). Adjust oscilloscope A POSITION control until peak of high pulse is at a horizontal reference line.

(u) Observe negative pulse with least amplitude (low pulse) and adjust test set SUM ATTEN until peak of low pulse reaches horizontal reference line. SUM ATTEN control setting change should be less than 1 dB.

g. Input Rf Power Measurement Adjustment

(1) *Test equipment required.*

(a) Signal Generator AN/USM–213
(b) Oscilloscope AN/USM-281A
(c) Interrogator Set AN/TPX-50
(d) Power Supply PP-2953A
(e) Test Facilities Set AN/TPM-24(V)3
(f) Pulse Generator AN/UPM–15A
(g) Differential Voltmeter ME-202/B/U
(h) Pulse Power Calibrator Set AN/UPM-73
(i) 10K ohm resistor

(2) *Adjustment procedure.*

(a) Connect test set up as shown in figure 3–11.

(b) Set up test set, paragraph 3–4 *b*, except set DE MOD VID LEVEL fully CCW and MEASUREMENT FUNCTION SEL to PWR.

(c) Set up pulse generator paragraph 3–4 *h* and adjust controls for a +20 volt pulse with a duration of 7 µsec. Then set pulse generator for external triggering.

(d) Set up signal generator, paragraph 3–4 *j* and set the controls as follows:

Control	*Position*
FREQUENCY	1030 MHz
ATTENUATOR	0.00 DB
ON/OFF	Pressed
RF	Pressed
ALC	Released
SQ WAVE	Released
PULSE	Pressed
AM	Released
FM	Released

(e) Note actual attenuation of 15 dB attenuator (marked on attenuator) connected to test set LOW PWR IN jack. Use following formula to calculate rf signal generator output.

$$\text{Signal generator output (dBm)} = \left(\begin{array}{c}\text{actual}\\ \text{attenuator}\\ \text{attenuation}\end{array}\right) - 12\text{dB}$$

i.e., +3.1 dBm = 15.1 dB -12dB.

NOTE

This is done to apply -12 dBm to test set LOW PWR IN jack.

(f) Set Up pulse power calibrator, paragraph 3–4 *k*, and the specific operating instructions (for internal trigger) described in TM 11 –6625–402–15. Set final setting of pulse power calibrator CALIBRATED ATTENUATOR control to generator output (dBm) calculated in *(e)* above.

(g) Adjust rf signal generator ATTENUATION (dB) control until output pulse observed on pulse calibrator set is at level of reference line. RF signal generator is now set for an output that provides a signal level at pulse power calibrator R.F. INPUT jack of the same value calculated in *(e)* above.

(h) Set pulse power calibrator set TRIGGER NO. 1 switch to OFF.

NOTE

Make sure 15 dB attenuator is installed on test set LOW PWR IN jack before performing step *(i)*.

(i) Disconnect rf cable from pulse power calibrator set R.F. INPUT jack and connect to 15 dB attenuator on test set LOW PWR IN jack.

(j) Install a 10K ohm resistor from M1A1TP1 to TP2.

(k) Connect differential voltmeter (+) probe to M1A1TP2 and (-) probe to GND.

(l) Adjust M1A1R1 (fig. 3–6) until differential voltmeter indicates 0.00 volts.

(m) Disconnect 10K ohm resistor and differential voltmeter applied in steps *(j)* and *(k)* from M1A1TP1 and TP2.

(n) Set pulse power calibrator set TRIGGER NO, 1 switch to ON, to apply rf to test set.

(o) Adjust DEMOD VID LEVEL for 1.0 VOLT display on oscilloscope.

(p) Adjust oscilloscope controls to view pulse.

(q) Adjust M1A1R2 (fig. 3–6) until MEASUREMENT meter indicates 18 dbw.

(r) Set pulse power calibrator set TRIGGER NO. 1 switch to OFF.

(s) Disconnect rf cable from 15 dB attenuator and connect it to pulse power calibrator set R.F. INPUT jack.

(t) Set pulse power calibrator TRIGGER NO. 1 switch to ON.

(u) Using pulse power calibrator set adjust rf signal generator output to +3.0 dBm as follows:

1 Set pulse power calibrator set CALIBRATED ATTENUATOR control to +3 dBm (030 + DB).

2 Adjust rf signal generator ATTENUATION (DB) control until output pulse observed on pulse power calibrator set is at level of reference line.

(v) Set pulse power calibrator set TRIGGER NO. 1 switch to OFF.

(w) Remove 15 dB attenuator from test set LOW PWR IN jack.

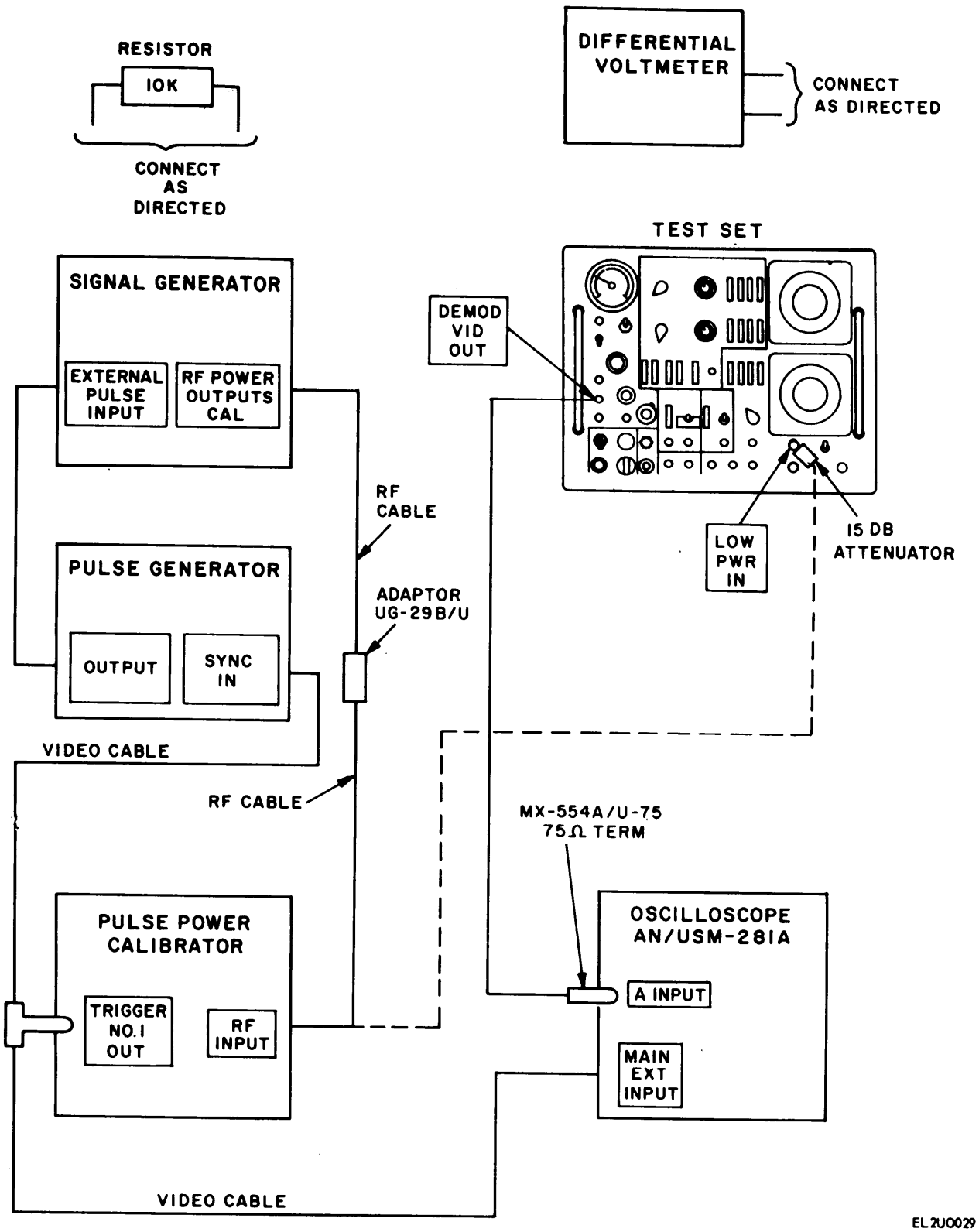


Figure 3-11. Power measurement adjustment setup.

(x) Disconnect rf cable from pulse power calibrator set R.F. INPUT and connect it directly to test set LOW PWR IN jack. Set pulse power calibrator set TRIGGER NO. 1 switch to ON.

(y) Adjust DEMOD VID LEVEL for 1.0 volt display on oscilloscope.

(z) Adjust M1A1R7 until MEASUREMENT meter indicates 33 dBw.

(aa) Set pulse power calibrator set TRIGGER NO. 1 switch to OFF.

(ab) Reconnect equipment as shown in figure 3– 11 and repeat steps *(f)* through *(i)* and *(n)* through *(aa).*

(ac) Connect test setup as shown in figure 3– 11 except do not connect 15 dB attenuator to the test set LOW PWR IN jack. Using pulse power calibrator set, set signal generator rf output to 0 dBm as follows:

1 Set pulse power calibrator set TRIGGER NO. 1 switch to ON.

2 Set pulse power calibrator set CALIBRATED ATTENUATOR control to 0 dBm (000 -DB).

3 Adjust rf signal generator ATTENUATION (DB) control until output pulse on pulse power calibrator set is at level of reference line.

(ad) Set pulse power calibrator set TRIGGER NO. 1 switch to OFF.

(ae) Disconnect rf cable from pulse power calibrator set R.R. INPUT jack and connect it directly to test set LOW PWR IN jack.

(af) Set pulse power calibrator set TRIGGER NO. 1 switch to ON.

(ag) Adjust DEMOD VID LEVEL for 1.0 volt display on oscilloscope. Observe MEASUREMENT meter indicates 30 ±1 dBw. If meter indication is not in tolerance, repeat steps *(e)* through *(ag)* except use different values (within ±1 dB) for MEASUREMENT meter indications stated in steps *(q)* and *(z).*

Example: If indication is too high, use values from 17.0 to 18.0 dBw in step *(q)* and/or 32.2 to 33.0 dBw for step (z). If indication is too low, use values of 18.0 to 18.8 dBw in step *(q)* and/or 33.0 to 34.0 dBw for step (z).

(ah) Perform procedure described in table 3–32, steps 1 thru 3. If performance standards are met proceed to step *(ak).* If performance standard is not met, continue with step *(ai).*

(ai) With equipment setup in table 3–32, step 3, adjust DEMOD VID LEVEL control until MEASUREMENT meter indicates output power recorded in table 3–32, step 1.

(aj) Adjust AR2C2 until pulse (displayed on oscilloscope) is 1.0 volts in amplitude.

(ak) Perform procedure described in table 3–32, steps 4 and 5 if performance standard is met, adjustment is complete. If standard is not met continue with step *(al).*

(al) With equipment set up as in table 3–32, step 5, adjust DEMOD VID LEVEL control until MEASUREMENT meter indicates power level recorded in table 3–32, step 1.

(am) Adjust AR2C8 until pulse (displayed on oscilloscope) is 1.0 volts in amplitude.

h. PRF Input Measurement Adjustment

(1) *Test equipment required.*

(a) Oscilloscope AN/USM-281A

(b) Frequency Counter AN/USM–207A

(2) *Adjustment procedure.*

(a) Connect test setup as shown in figure 3–12.

(b) Set up test set, paragraph *3–4b* except set MEASUREMENT FUNCTION SEL switch to PRF EXT.

(c) Set Up oscilloscope, paragraph 3–4c and as follows:

Control	*Setting*
A VOLTS/DIV	0.05
MAIN SLOPE	
MAIN TIME/DIV	10µSEC
MAIN EXT ÷ 10/EXT/INT/LINE	INT

(d) Set up frequency counter, paragraph 3–4e and as follows:

Control	*Position*
SENSITIVITY	FREQ C
FUNCTION	FREQ
Time base	1
COM/SEP	SEP
C MULTIPLIER	3
C TRIGGER VOLTS	0
C SLOPE	+

(e) Connect 10X probe (oscilloscope A INPUT) to A10TP3.

(f) Adjust A10R27 until slope duration is 99 µsec (B, figure 3–15). Remove probe from A10TP3.

(g) Adjust PRT SELECT switches until frequency counter indicates 2 KHz and adjust A10R16 until test set MEASUREMENT meter indicates 2 on Hz scale.

(h) Adjust test set PRT SELECT (µ3EC) switches until frequency counter indicates 1 KHz.

(i) Set test set MEASUREMENT PRF RANGE switch to X100.

(j) Adjust A10R20 until test set MEASUREMENT meter indicates 10.

(k) Adjust test set PRT SELECT (µSEC) switches until frequency counter indicates 100 Hz.

(l) Observe that test set MEASUREMENT meter indicates 1±5%.

(m) Set test set MEASUREMENT PRF RANGE switch to X10.

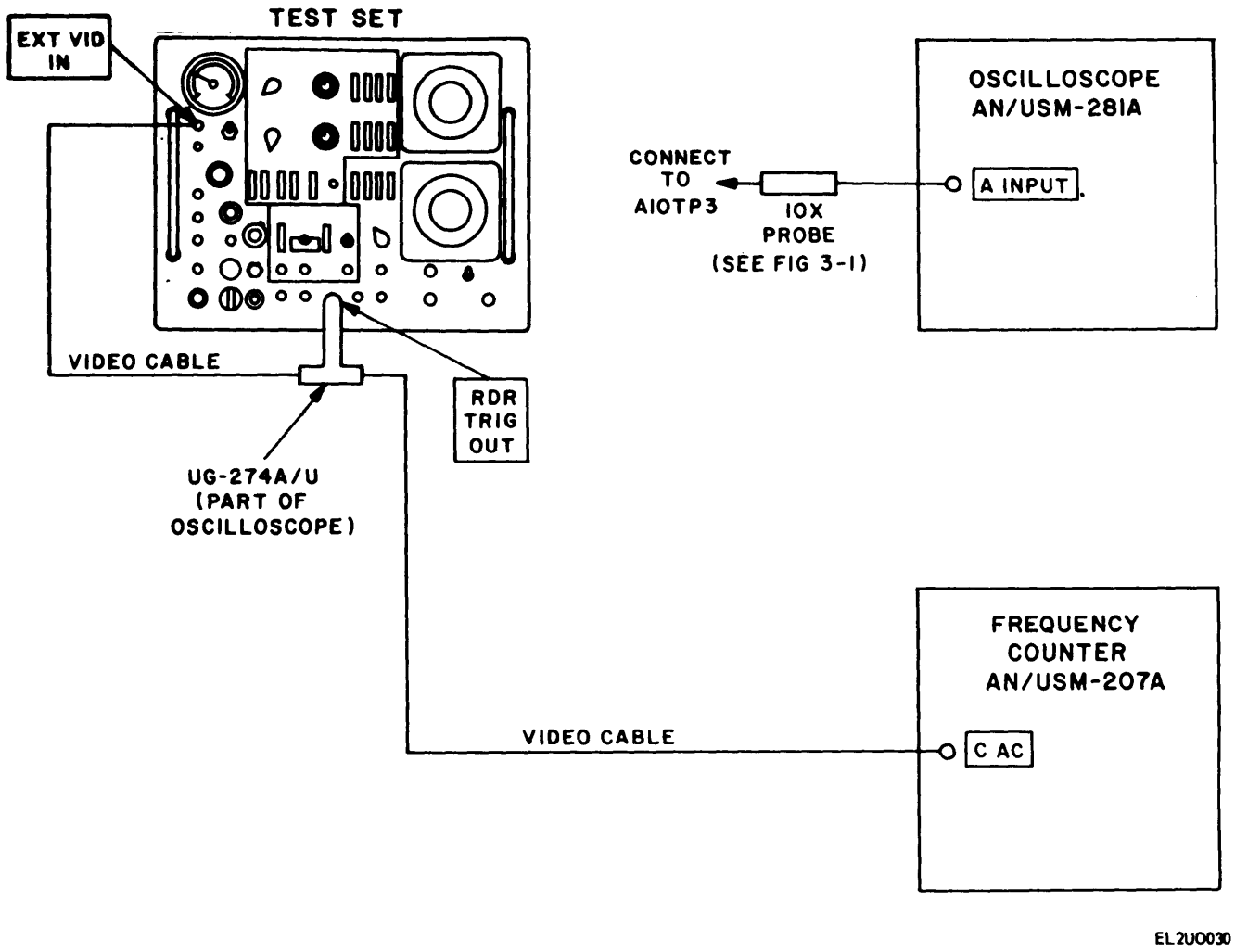


Figure 3-12. Prf input measurment adjustment setup.

(n) Adjust A10R24 until test set MEASUREMENT meter indicates 10.

i. Reply Nominal Delay and SIF Pretrigger Delay

(1) *Test equipment required.*

(a) Oscilloscope AN/USM–281A

(b) Frequency Counter AN/USM–207A

(2) *Adjustment procedure.*

(a) Connect test set up as shown in figure 3-13.

(b) Set oscilloscope controls as in table 3–2, except set DISPLAY switch to ALT, A VOLTS/DIV to 5, and B VOLTS/DIV to 10.

(c) Set test set controls as in table 3–1 except set PRT SEL (µSEC) switches to 2500.

(d) Set up frequency counter, paragraph 3–4 *e* and set controls as follows:

Control	Position
FUNCTION	TIME B-C
Time base	107
B and C MULTIPLIER	3
B and C TRIGGER VOLTS	+2
B and C SLOPE	+

(e) Observe radar trigger pulse on A input and SIF pre trigger on B input on oscilloscope,

(f) Adjust A1S7, S8 and S9 (fig. 3–14) for delay reading of 386.0 ±0.5 µsec on frequency counter.

NOTE

The SIF pre trigger delay is adjustable in steps of 0.1 µsec from 301.0 to 398.0 µsec from radar trigger using A1S7, S8, S9.

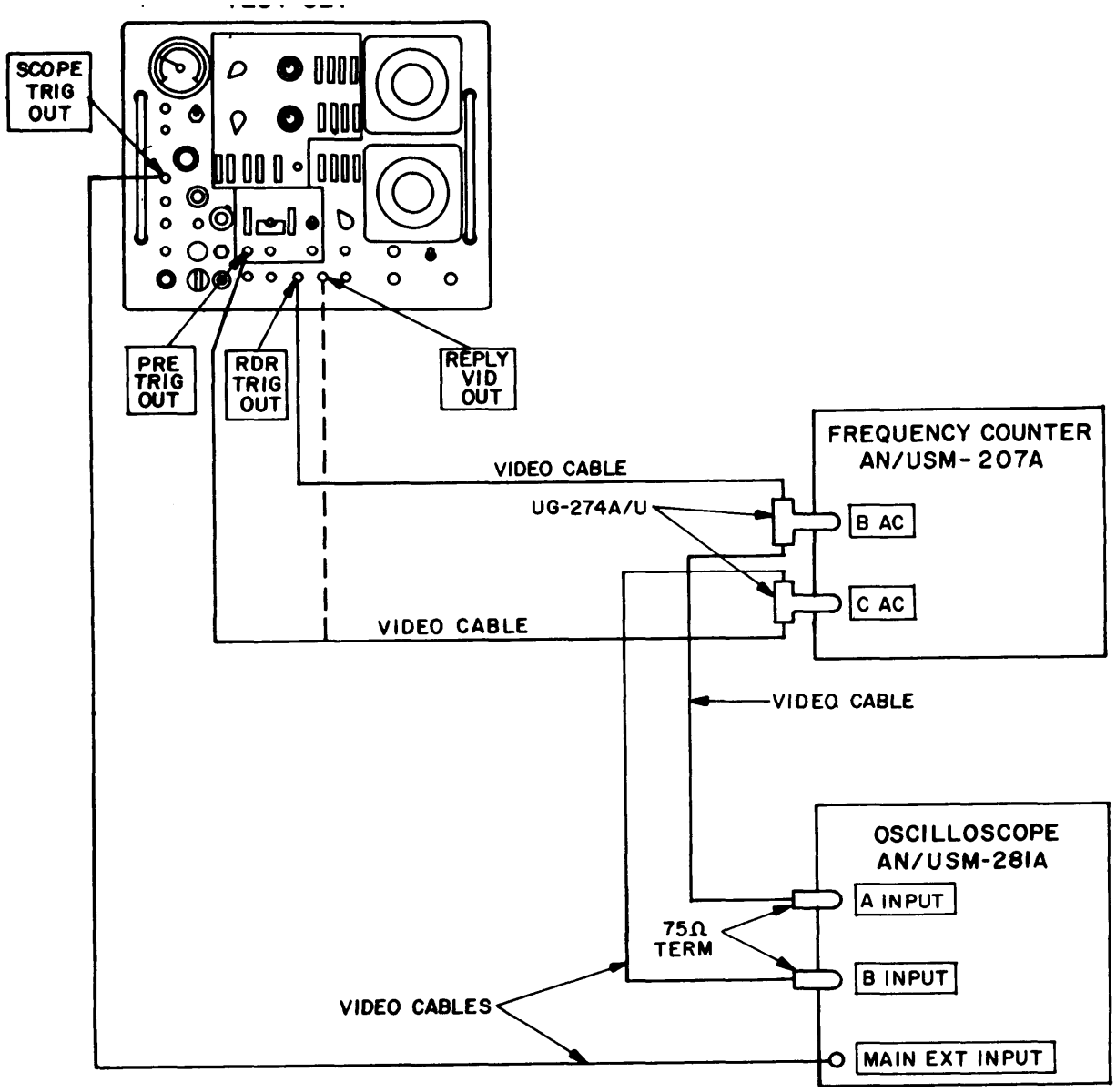


Figure 3–13. Reply nominal delay and SIF pretrigger delay adjustment setup.

(g) Remove cable from test set PRE TRIG OUT jack and connect to REPLY VID OUT jack.

(h) Adjust oscilloscope controls to observe radar trigger on A INPUT and SIF REPLIES and B INPUT.

(i) Adjust A1S4, S5, and S6 for delay of 434.0 ±0.5 µsec (on frequency counter) from radar trigger to F1 pulse of reply train.

NOTE

The SIF reply video delay is adjustable in steps of 0.1 µsec from 360.0 to 438.0 µsec from radar trigger using A1S4, S5, and S6.

(j) Set test set REPLIES MODULATION SEL switch to M4–3P.

(k) Adjust oscilloscope controls to observe

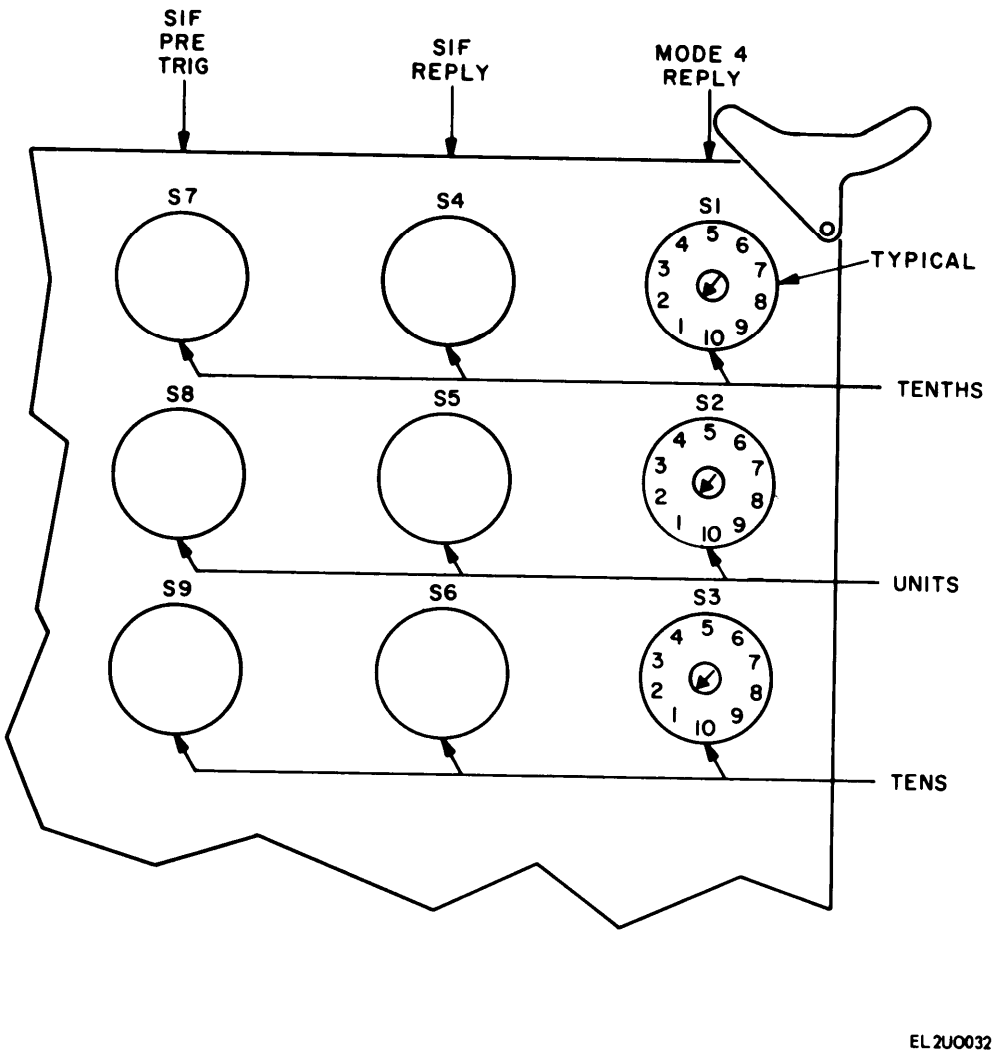


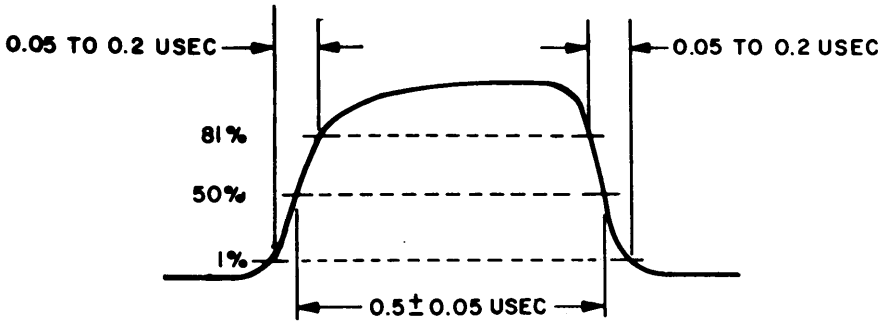
Figure 3–14. Circuit card A1 switch location diagram.

radar trigger on A INPUT and Mode 4 reply video on B INPUT.

(l) Adjust A1S1, S2 and S3 for delay of 449.0 ±0.6 µsec (on frequency counter) from radar trigger to first mode 4 reply video pulse.

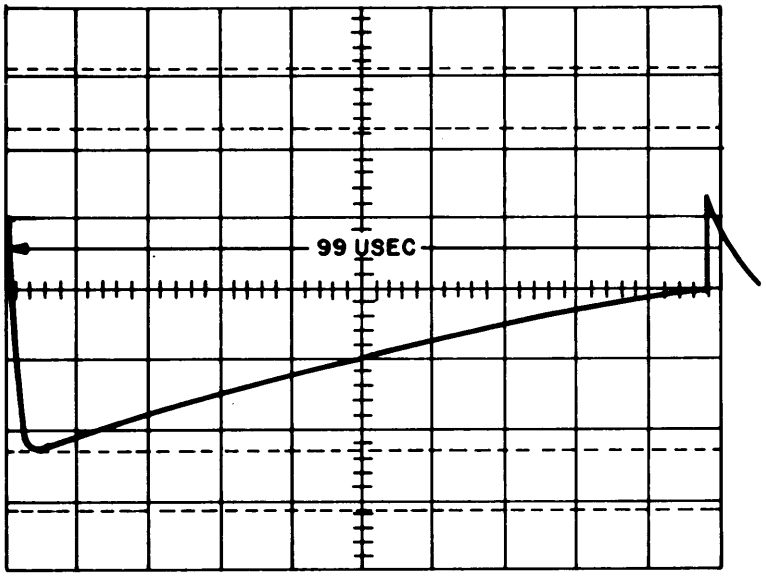
NOTE

The mode 4 reply video is adjustable in steps of 0.1 µsec from 430.5 to 464.5 µsec from radar trigger using A1S1, S2, and A1S3.



A. DETECTED RF OUTPUT PULSE TOLERANCES

TEST POINT A1OTP3
10X PROBE–A INPUT



A VOLTS/DIV	.05
DISPLAY	A
SWEEP DISPLAY	MAIN
MAIN TIME/DIV	10 USEC
MAIN EXT ÷ IO/EXT/INT/LINE	INT
MAIN SLOPE	

B. MEASUREMENT PULSE DURATION

EL2W033

Figure 3–15. Adjustment waveforms.

Section V. REPAIR

3 – 11. Parts Replacement Techniques

All parts are easily accessible and can be replaced without special procedures. The following general precautions apply to the equipment:

a. Use the pencil type 55-watt soldering iron supplied with Tool Kit Electronic Equipment TK–105/G for removal and repair of chassis mounted components. If the iron is to be used with alternating current, use an isolating transformer between the soldering iron and the line. Do not use a soldering gun; damaging voltages can be induced in components.

b. When soldering transistor or diode leads, solder quickly; whenever wiring permits, use a heatsink (such a long-nosed pliers) between the soldered joint and the transistor or diode. Use approximately the same lead length and dress as used originally.

c. Wiring diagram information in figure FO–20 should be referred to as required to ensure correct part replacements.

3 – 12. Parts Substitution

Do not substitute parts indiscriminately. Substitute parts only when the trouble has been isolated to a specific stage and the defective part has been localized.

Section VI. GENERAL SUPPORT TEST PROCEDURES

3 – 13. Purpose and Instructions

a. Test procedures contained in table 3–3 are to be used for general support maintenance to determine the acceptability of repaired equipment. The procedures listed in paragraph 3 – 15 are functional test procedures. Once equipment is repaired, the test set should be tested using these procedures.

b. Separate functional test procedures are given to check various sections of the test set so that only the section repaired is tested. Performing all the functional test procedures given in the order given will provide a complete test of the test set should it be required.

c. Perform each functional test procedure in sequence; do not vary the sequence. For each step, perform all the actions required in the control settings column; then perform each specific test procedure and verify it against the performance standard. If a fault is noted, locate malfunction in table 3–4 which most describes symptoms of fault.

3 – 14. Test Equipment Required for Testing

All test equipment required to perform the testing procedures of this section is listed in paragraph 3 –4, Power input connections to the test set and the test equipment are not shown on the test setup figures unless they are part of the test procedure.

3 – 15. Test Procedures

General support test procedures are listed below.

a. Overall Inspection Procedure, table 3–6.
b. Power Supply Performance Test, table 3–7.
c. Radar Trigger Functional Test, table 3–8.
d. Scope Trigger Functional Test, table 3–9.
e. SIF Pretrigger Functional Test, table 3–10.
f. External Gating Functional Test, table 3-11.
g. External Modulation Functional Test, table 3–12.
h. Timing Markers Functional Test, table 3– 13.
i. 30 KHZ Functional Test, table 3–14.
j. Interleave Functional Test, table 3–15.
k. BIT Frequency Self Test Functional Test, table 3–16.
l. Delayed Rf Sweep Trigger Functional Test, table 3–17.
m. Sweep Frequency Mode PRF Countdown Functional Test, table 3–18.
n. Decode Functional Test, table 3– 19.
o. SIF Challenge Video Functional Test, table 3–20.
p. Pulse Repetition Functional Test, table 3–21.
q. Pulse Repetition Measurement Functional Test, table 3–22,
r. External Trigger Input Functional Test, table 3–23.
s. Range Delay Functional Test, table 3–24.
t. SIF Reply and Substitute Pulse Spacing Functional Test, table 3–25.
u. Mode 4 Reply Functional Test, table 3–26.
v. Variable Gating Functional Test, table 3–27.
w. Mode 4 Challenge Video and GTC Trigger Functional Test, table 3–28.
x. Rf Output Frequency Functional Test, table 3–29.
y. Rf Output Power Functional Test, table 3–30.
z. Modulator and Demodulator Functional Test, table 3–31,
aa. Rf Input Power Functional Test, table 3–32.
ab. Rf Input Frequency Measurement Functional Test, table 3–33.

Table 3–6. Overall Inspection Procedure

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1		POWER switch: OFF.	Inspect all controls and mechanical assemblies for loose or missing screws, nuts, and bolts.	Screws, nuts, and bolts must be tight; none missing.
2			Inspect all connectors, sockets, and receptacles for looseness and damage.	No looseness or damage evident.
3			Inspect plugs, connectors, control knobs, and control panel for cleanliness.	All items must be free of dust or dirt. If cleaning is required, refer to TM 11–6625–2610–12.
4			Inspect all cable assemblies for signs of mechanical damage, such as chafed, cracked, or frayed insulation.	All cables must be free of chafed, cracked and frayed insulation.
5			Inspect gasket of control panel for looseness, deterioration or damage.	Observe that the gasket is tight, resilient, and free from cuts or tears.

Table 3–7 Power Supply Performance Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–16.	POWER switch OFF.	Adjust transformer until voltmeter indicates 115 vac.	
2	Set up differential voltmeter, paragraph *3–4d*.	POWER switch: ON.	*a.* Observe POWER 1.5 AMP fuseholder. *b.* Observe POWER indicator. *c.* Observe DC FAULT indicator. *d.* Press DC FAULT indicator.	*a.* Fuseholder is extinguished. *b.* POWER indicator is lit. *c.* DC FAULT indicator is extinguished. *d.* DC FAULT indicator lights.
3	**NOTE** During steps 3 through 6, use measurement of dc voltage procedure described in TM 11–6625–537-15, to obtain differential voltmeter indication.		*a.* Connect differential voltmeter between PS1A1TP1(+) and ground (fig. 3– 1). Observe differential voltmeter indication. *b.* Adjust transformer until multimeter indicates 103.5 volts. Observe differential voltmeter indication. *c.* Adjust transformer until multimeter indicates 126.5 volts. Observe differential voltmeter indication.	*a.* Differential voltmeter indicates 27.75 to 28.25. *b.* Differential voltmeter indicates 27.75 to 28.25 volts. *c.* Differential voltmeter indicates 27.75 to 28.25 volts.
4	Differential voltmeter: NULL switch: VTVM.		*a.* Connect differential voltmeter between PS1A1TP5(+) and ground (fig. 3–1). Observe differential voltmeter indication. *b.* Adjust transformer until multimeter indicates 103.5 volts. Observe differential voltmeter indication.	*a.* Differential voltmeter indicates 11.75 to 12.25 volts. *b.* Differential voltmeter indicates 11.75 to 12.25 volts.

Table 3–7. Power Supply Performance Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
5	Differential voltmeter: NULL switch: VTVM.		*a.* Connect differential voltmeter negative probe to PS1A1TP6(-) and positive probe to ground (fig. 3-1). Observe differential voltmeter indication. *b.* Adjust transformer until voltmeter indicates 126.5 volts. Observe differential voltmeter indication.	*a.* Differential voltmeter indicates 11.75 to 12.25 volts (-voltage). *b.* Differential voltmeter indicates 11.75 to 12.25 volts (-voltage).
6	Differential voltmeter: NULL switch: VTVM.		*a.* Connect differential voltmeter positive probe to PS1A1TP7(+) and negative probe to ground (fig. 3-1), Observe differential voltmeter indication. *b.* Adjust transformer until voltmeter indicates 103.5 volts. Observe differential voltmeter indication.	*a.* Differential voltmeter indicates 4.75 to 5.25 volts. *b.* Differential voltmeter indicates 4.75 to 5.25 volts.

Table 3–8. Radar Trigger Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–17. Set up oscilloscope, paragraph 3–4c except: A VOLTS/DIV switch: 2. DELAYED TIME/DIV switch: .5 µSEC.	Set up test set, paragraph *3–4b*.	Adjust oscilloscope controls to observe radar trigger pulse.	*a.* Amplitude is +10.0 ±1.0 volt. *b.* Width is 3.0 ±1.0 µsec.

Table 3–9. Scope Trigger Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–17 except disconnect video cable and 75Ω termination on A INPUT.	Set up test set, paragraph *3–4b*.	Adjust oscilloscope controls to observe scope trigger pulse.	*a.* Amplitude is 5.0 ±1.0 volt. *b.* Width is 1.0 to 5.0 µsec.

Table 3–9. Scope Trigger Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
(cont.)	Disconnect video cable on MAIN EXT and connect with 93Ω termination on A INPUT. Set up oscilloscope, paragraph 3–4 *c* except: MAIN TIME/DIV switch: .5 µSEC. MAIN EXT ÷ 10/ EXT/INT/LINE switch: INT.			

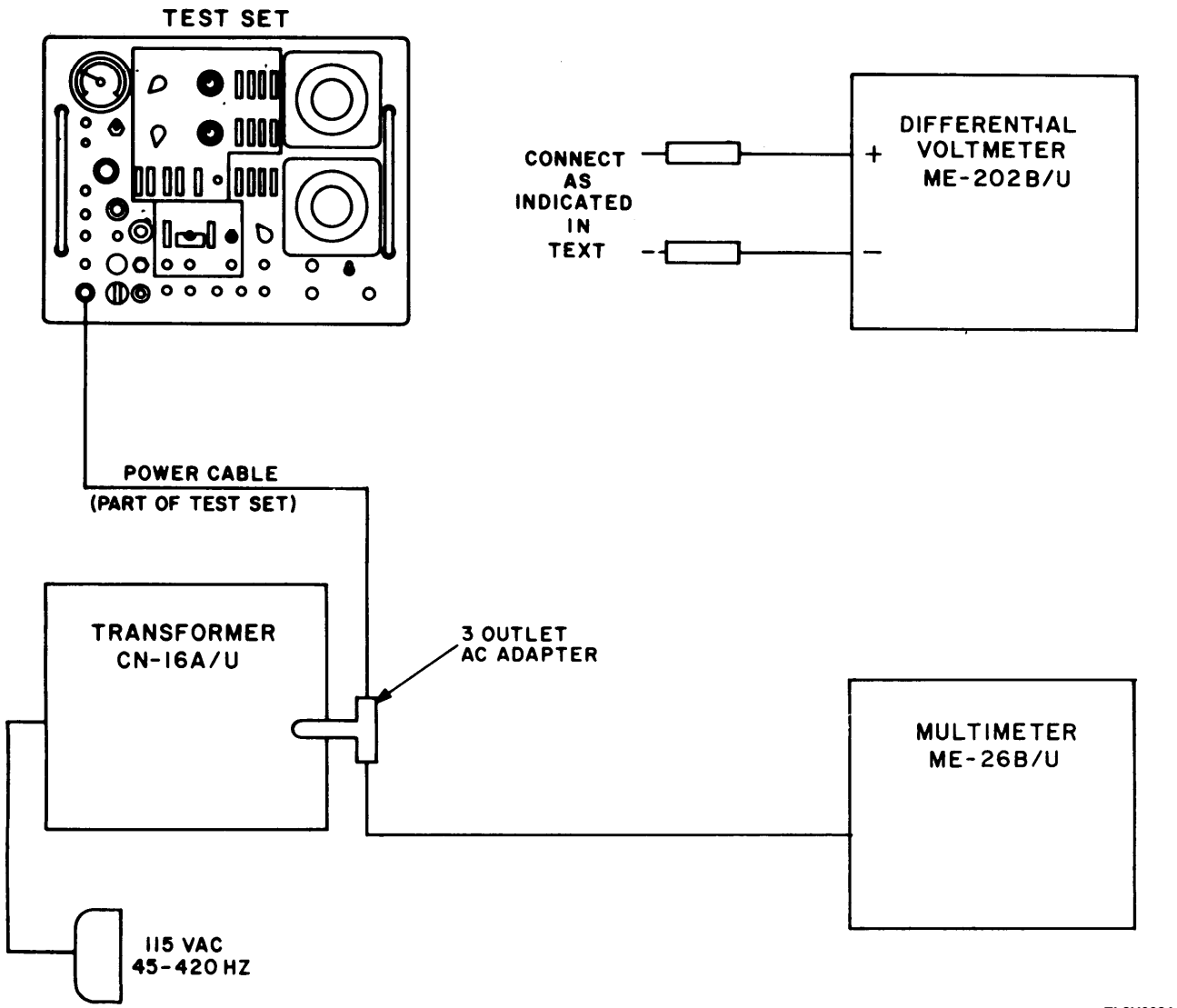


Figure 3–16. Power supply test setup.

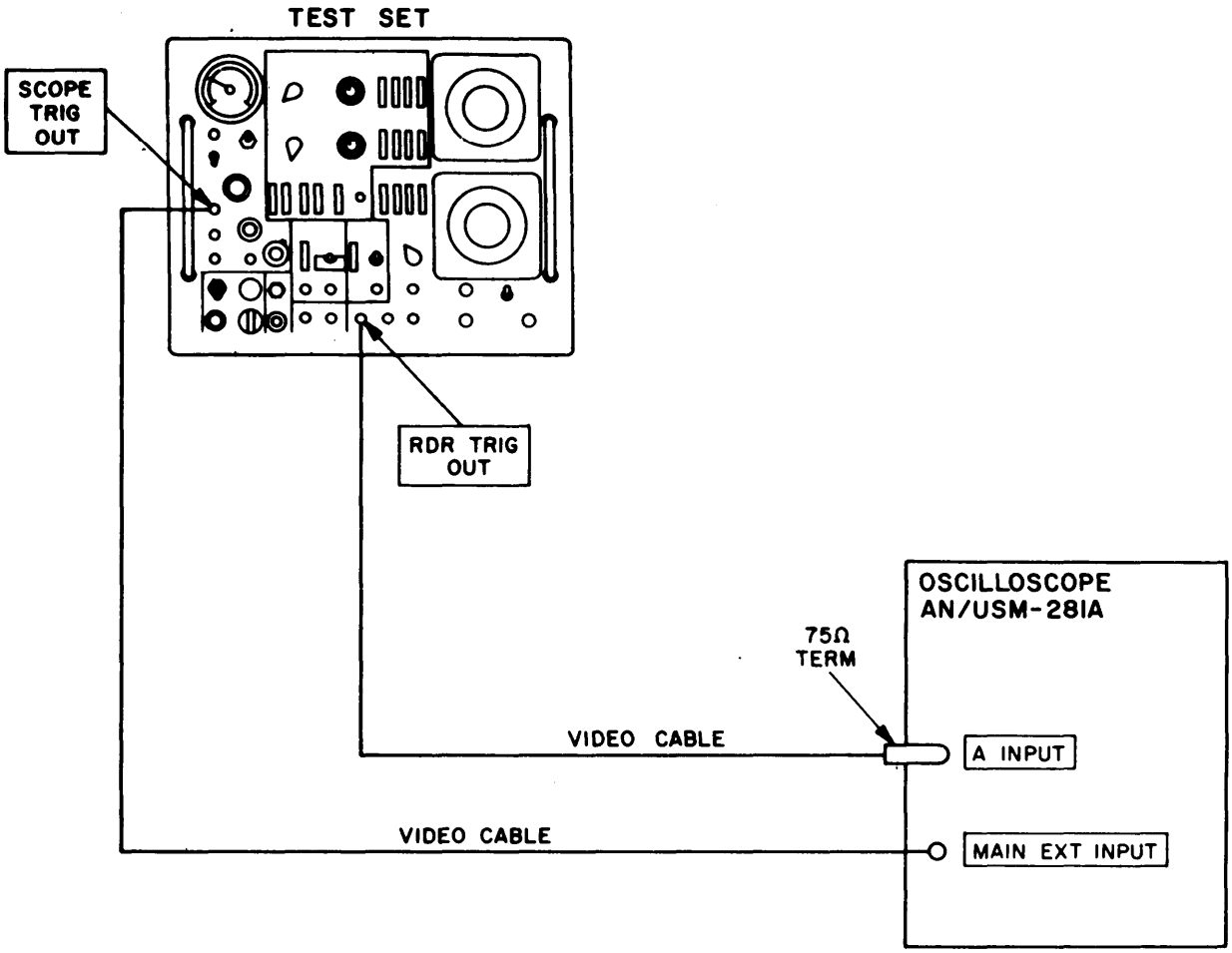


Figure 3–17. Radar trigger and scope trigger characteristics test setup.

Table 3–10. SIF Pretrigger Functimal Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test set up as shown in figure 3–18. Set up oscilloscope, paragraph 3–4c except: MAIN TIME/DIV switch: 50 µSEC. A and B VOLTS/DIV switch: 5. DISPLAY switch: ALT.	Set up test set, paragraph *3–46.*	*a.* Adjust oscilloscope controls to observe delay from radar trigger on A INPUT to SIF pretrigger on B INPUT. *b.* Observe frequency counter indication.	*a.* None. *b.* Frequency counter indicates 386.0 ±0.5 µsec. **NOTE** 386.0 µsec is a nominal setting, delay is variable from 301 to 398 µsec in 0.1 µsec steps.

Tab/e 3–10. SIF Pretrigger Functimal Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (cont.)	Set frequency counter, paragraph 3–4e and as follows: Time base switch: 107. Mode selector switch: SEP. Function switch: TIME B-C. B and C SLOPE switches: +. B MULTIPLIER switch: 3. B TRIGGER VOLTS control: +2. C MULTIPLIER switch: 3. C TRIGGER VOLTS control: +2.			
2	Set oscilloscope DISPLAY switch: B. DELAYED TIME/DIV switch: .1 µSEC. Sweep display switch: DELAYED.		Adjust oscilloscope DIV DELAY control to observe sif pretrigger pulse.	*a.* Amplitude 20.0 ± 4.0 volts. *b.* Width 0.8 ± 0.1 µsec.

Table 3–1 1. External Gating Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–19.	Set up test set, paragraph *3–4b*.	*a.* Observe oscilloscope. *b.* Set voltage on DC POWER SOURCE for 5 volts. *c.* Connect DC POWER SOURCE (-) lead to test set ground connector and (+) lead to center pin of 75Ω termination on test set REPLY VID OUT jack.	*a. No* reply pulses present on oscilloscope. *c.* Reply pulses appear.

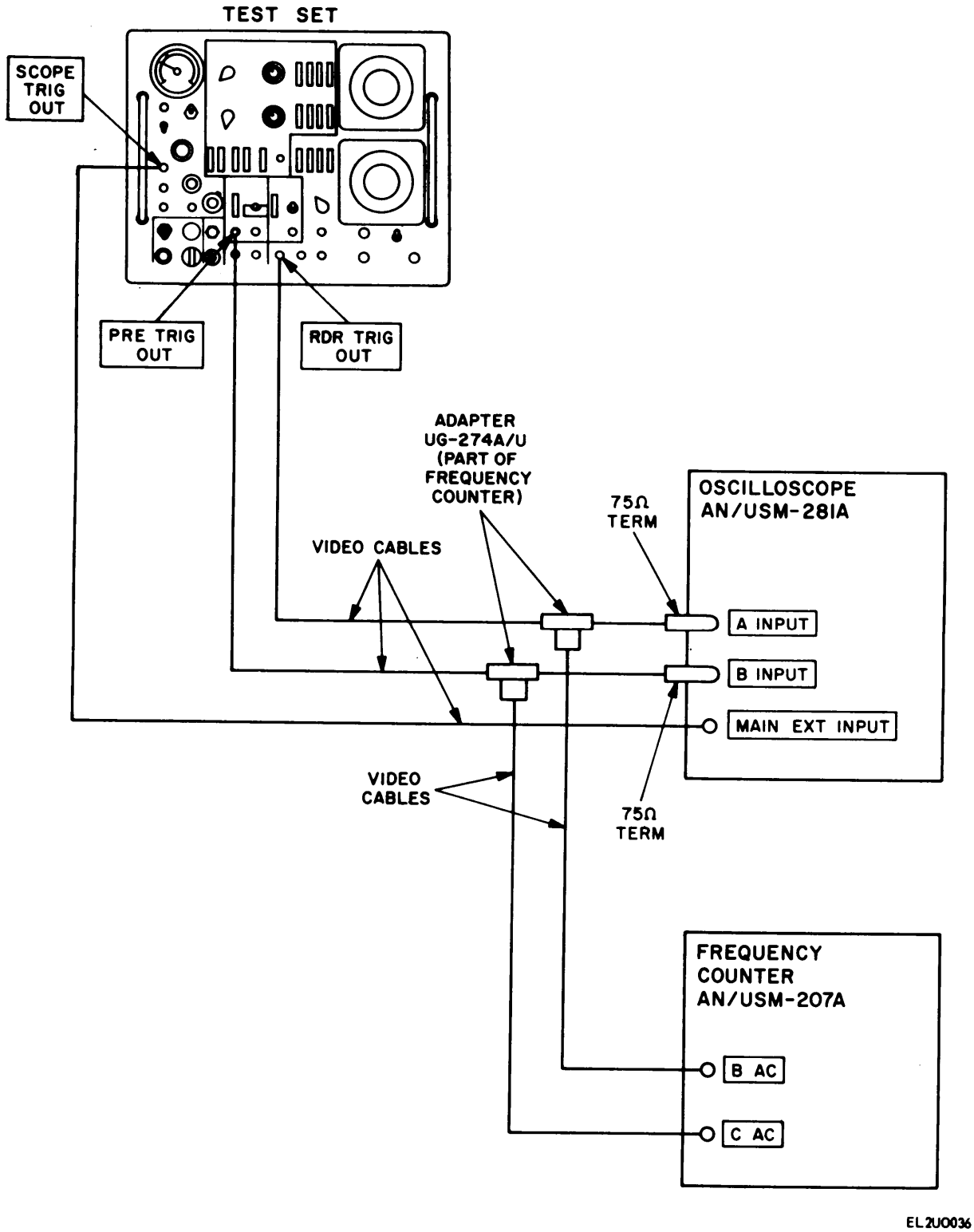


Figure 3-18. SIF pretrigger charateristics and timing test setup.

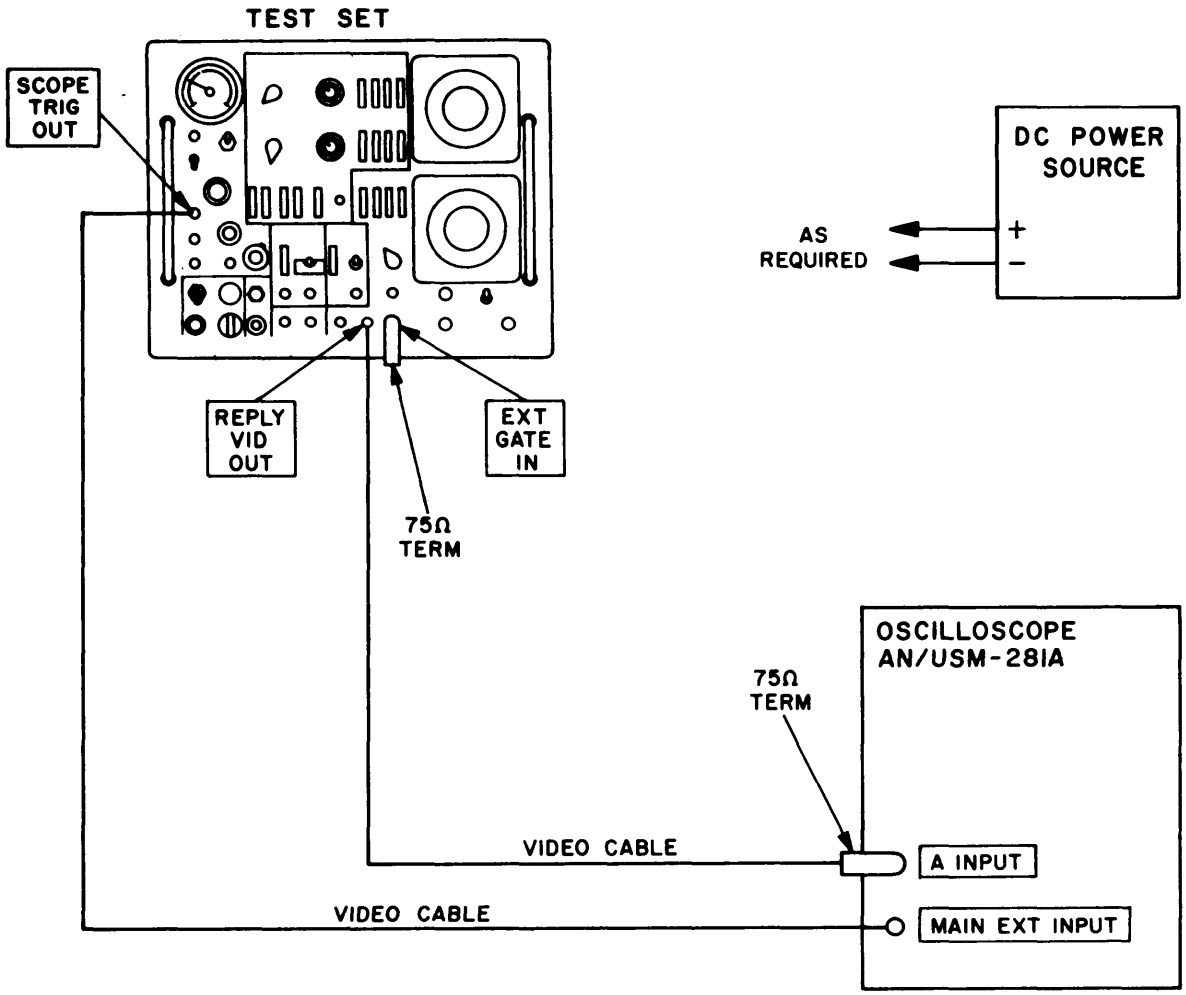


Figure 3-19. External gating test setup.

Table 3–12 External Modulation Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–20. Set up oscilloscope, paragraph 3–4c except: DELAYED TIME/ DIV switch: .1 µSEC. Set up pulse generator, paragraph *3–4h* and adjust as follows:	Set up test set, paragraph *3–4b* except: REPLIES MODULATION SEL switch: OFF.	*a.* Adjust pulse generator FINE ATTN control until pulses on oscilloscope A INPUT are 5 volts in amplitude. *b.* Adjust oscilloscope to observe one pulse on delayed sweep. *c.* Adjust pulse generator WIDTH control until pulse width is 0.5 µsec. *d.* Adjust pulse generator RISE TIME control until pulse rise time is <0.1 µsec.	

Table 3–12. External Modulation Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (cont.)	COARSE ATTEN switch: 1. FINE ATTN control: midrange PULSE NO. *2* switch: OUT. WIDTH switch: NAR. POLARITY switch: POS. SYNC switch: EXT GOING +. BIAS control: adjust until pulses appear on oscilloscope.			
2	Oscilloscope B VOLTS/DIV switch: 2. DISPLAY switch: ALT.	DEMOD VID LEVEL control: adjust until pulse on oscilloscope B INPUT is 1.0 volt amplitude.	*a.* Observe pulses on oscilloscope A and B INPUTS. *b.* Measure delay between pulses on oscilloscope A INPUT and B INPUT.	*a.* One pulse is present on B INPUT for each pulse on A INPUT. *b.* Delay does not exceed *0.3 µsec.*

Table 3–13. Timing Markers Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–21. Set up oscilloscope, paragraph 3–4c except: MAIN TIME/DIV switch: 20 µSEC. DELAYED TIME/ DIV switch: .1 µSEC. Sweep display switch: DELAYED. Set up frequency counter, paragraph *3–4c* and as follows: SENSITIVITY switch: FREQ C. C TRIGGER VOLTS switch: 1. Mode selector switch: SEP. FUNCTION switch: FREQ. Time base switch: 10. C TRIGGER VOLTS control: CCW.	Set up test set, paragraph 3–4b.	Adjust frequency counter C TRIGGER VOLTS control cw until steady reading is displayed.	Frequency counter indicates 10,000 KHz ±2 KHz (0.1 µsec).

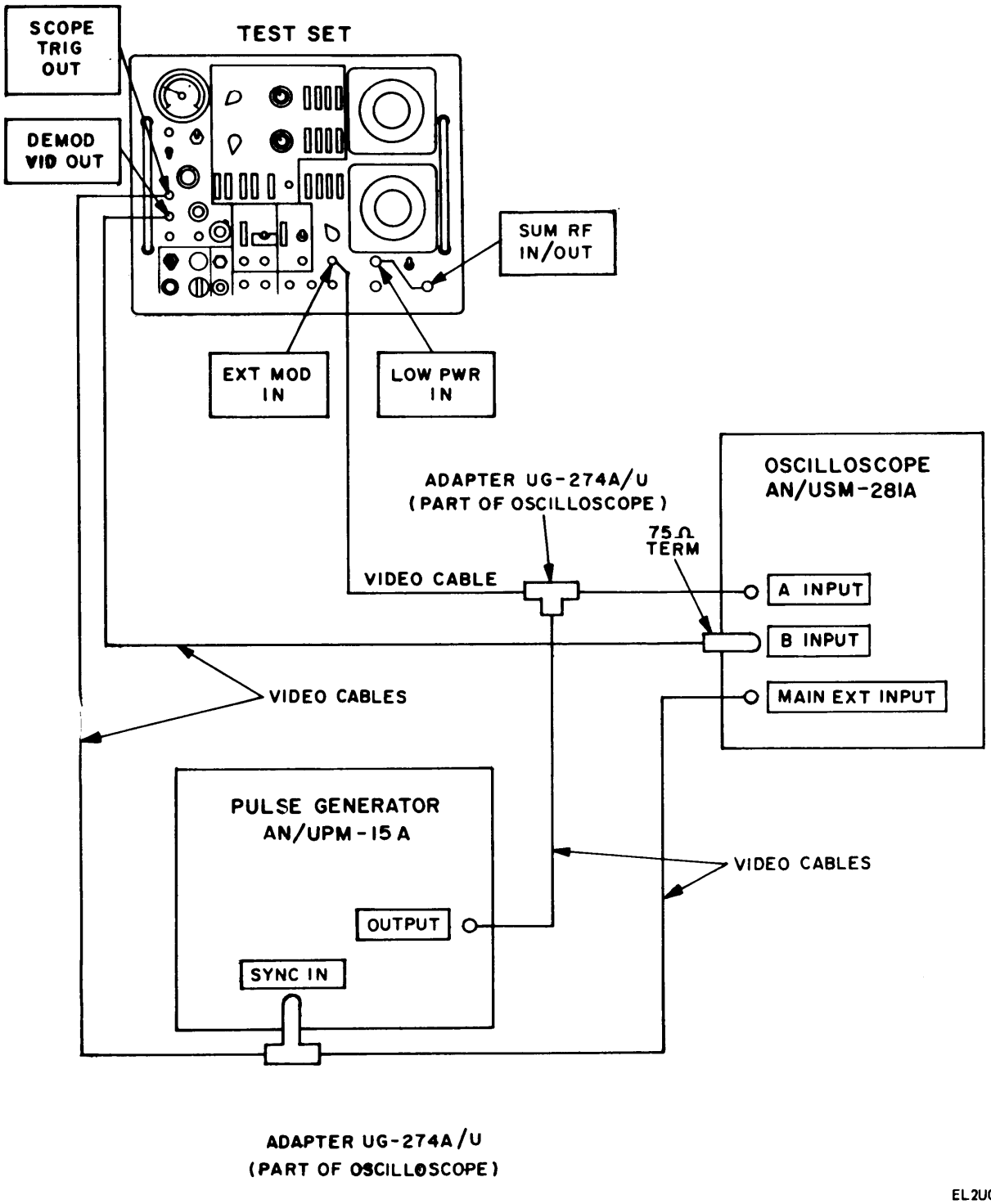


Figure 3–20. External modulalation test setup.

Table 3–13. Timing Markers Functional Test —Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
2			Observe four levels of markers.	Four levels of markers are present (0.1, 1.0, 10.0 and 100.0 µsec ±0.2%).
3			Measure spacing from leading edge to leading edge of lowest amplitude level of markers.	***a.*** Markers are spaced 0.1 ±sec apart. ***b.*** Marker amplitude is >0.5 volts.
4	Oscilloscope: DELAYED TIME/DIV switch: 1 µSEC.		Measure spacing from leading edge to leading edge of second level of markers.	Markers are spaced 1.0 µsec apart.
5	Oscilloscope: DELAYED TIME/DIV switch: 10 µSEC.		Measure spacing from leading edge to leading edge of third level of markers.	Markers are spaced 10.0 µsec apart.
6	Oscilloscope: DELAYED TIME/DIV switch: 100 µSEC.		Measure spacing from leading edge to leading edge of highest level of markers.	Markers are spaced 100.0 µsec apart.

Table 3–14. 90 KHz Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–22. Set up frequency counter, paragraph 3–4e and as follows: SENSITIVITY switch: 100 V. Time base switch: 10. FUNCTION switch: FREQ.	Set up test set, paragraph *3–4b* except: REPLIES MODULATION SEL switch: 30 KHZ.	Adjust frequency counter SENSITIVITY switch ccw until consistent readouts are displayed.	Frequency is ***30*** to *37* KHz.

Table 3–15. Interleave Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–23. Set up oscilloscope, paragraph 3–4c except:	Set up test set, paragraph *3–4b* except: SIG GEN NORM/INTERLEAVE switch: INTERLEAVE.	*a.* Adjust oscilloscope DIV DELAY control to observe interleaved pulse trains on A INPUT. *b.* Adjust test set MEASUREMENT DEMOD VID LEVEL control for 1.0 v amplitude.	Two interleaved pulse trains (4 pulses).

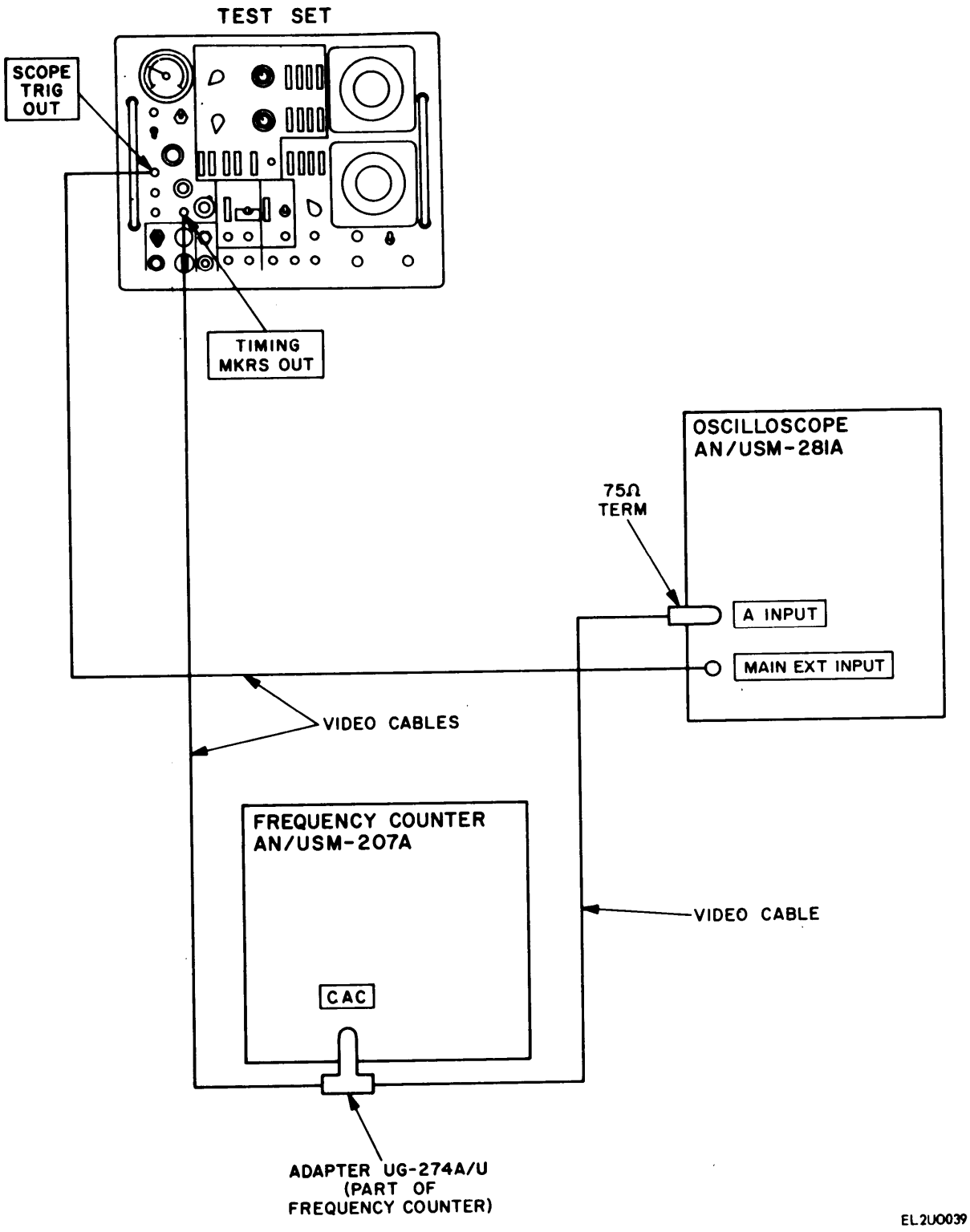


Figure 3-21. Timing markers test setup.

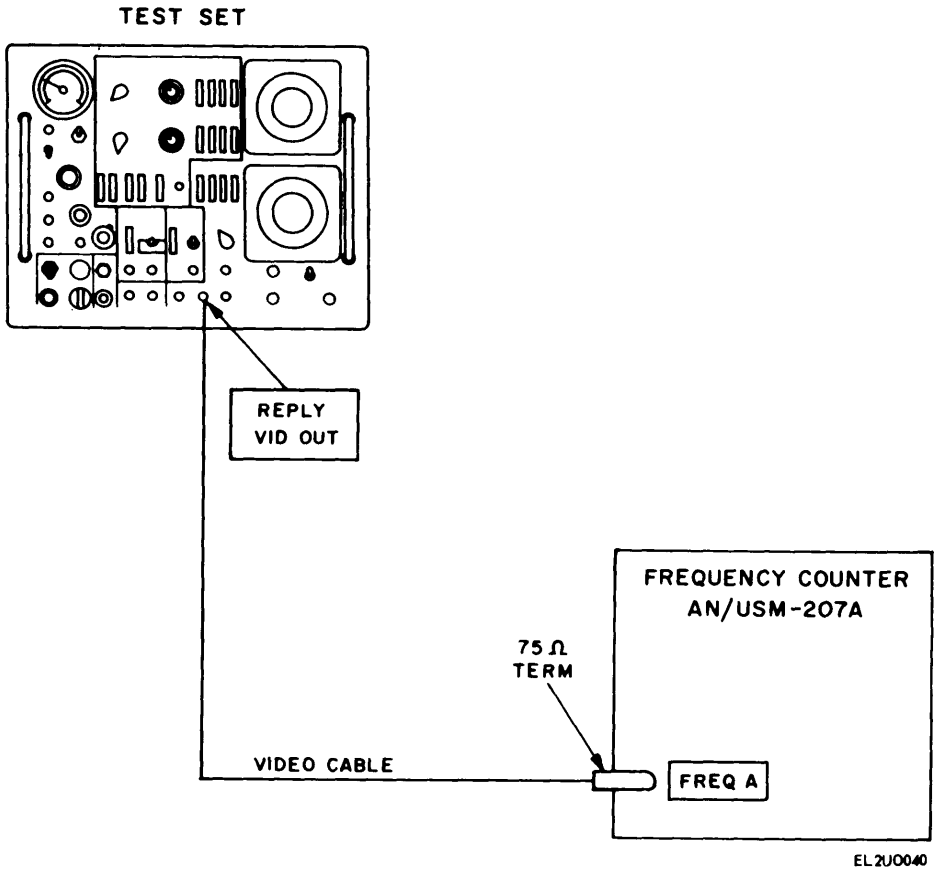


Figure 3–22. 30 KHz test setup.

Table 3–15. Interleave Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (cont.)	DELAYED TIME/DIV switch: 5 µSEC, Sweep display switch: DELAYED, A VOLTS/DIV switch: 5.	REPLIES REPLY WIDTH switch: 0.45. REPLIES SIF REPLY CODE switches: 0000. SUM ATTEN control: -1 DB.		
2	Oscilloscope: DELAYED TIME/DIV switch: .5 µSEC.		Adjust oscilloscope DIV DELAY control to observe spacing from the first pulse to the second pulse (interleaved pulse).	Pulse spacing is 0.70 ±0.05 µsec.
3			*a.* Adjust oscilloscope A INPUT POSITION control to reference peak first pulse.	*a.* None.
			b. Adjust test set SUM ATTEN control until peak of second pulse is at reference level of a, above.	*b.* Change of SUM ATTN control is within ±1.0 dB.

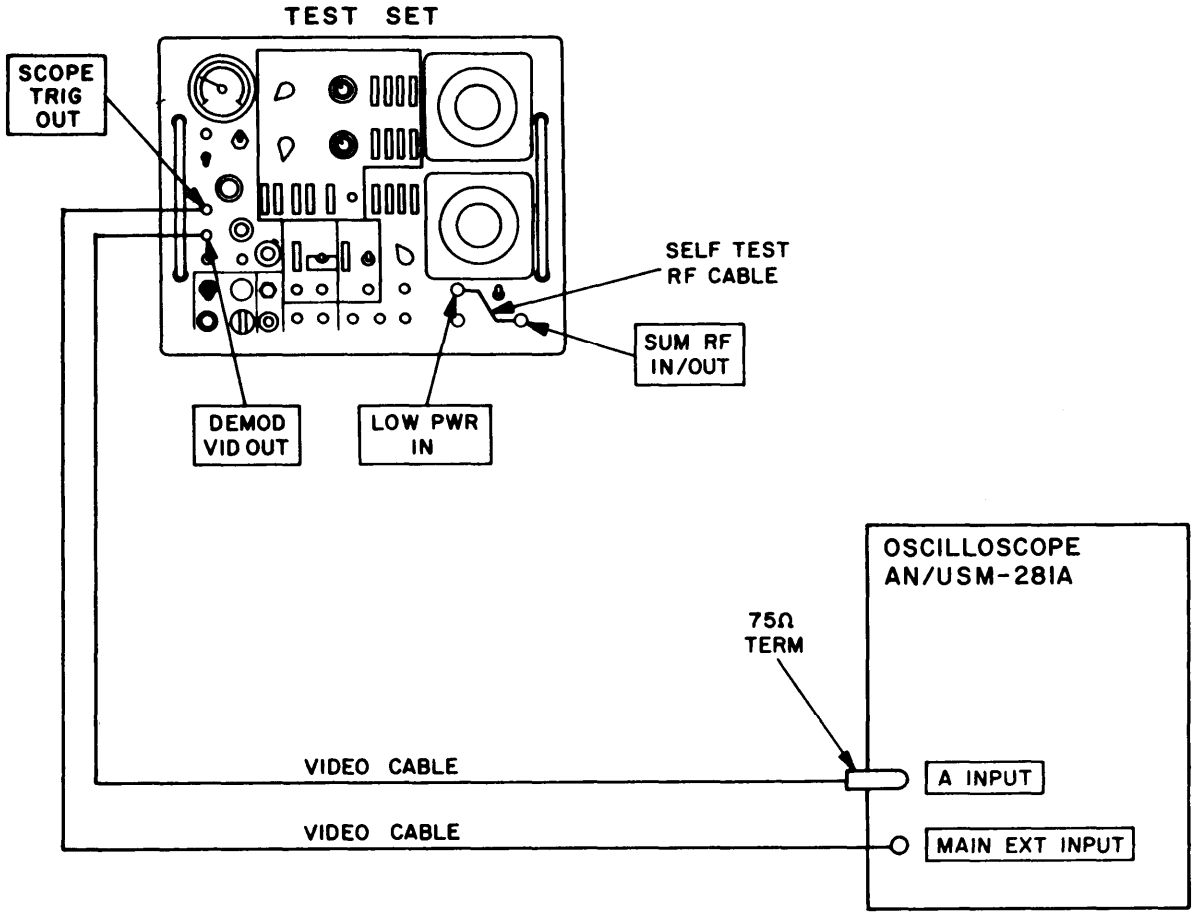


Figure-3-23 Interleave test setup

Table 3-16. BIT Frequency Self Test Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure *3–24.* Set up oscilloscope, paragraph *3–4c* except: DELAYED TIME/DIV switch: *20* uSEC. Sweep display switch: DELAYED. DISPLAY switch: ALT.	Set up test set, paragraph *3–4b* except: MEASUREMENT FUNCTION SEL switch: FREQ. MEASUREMENT DEMOD VID LEVEL switch: CCW. SIG GEN FUNCTION switch: SWP ±5 MHZ.	a. Adjust oscilloscope DIV DELAY control to observe -1, 0, and +1 MHz markers. *b.* Press test set BIT (MOM) switch and observe BIT frequency signal.	*a.* None. *b.* Peak of swept BIT frequency signal is within 0.3 MHz of center marker (1090 MHz).

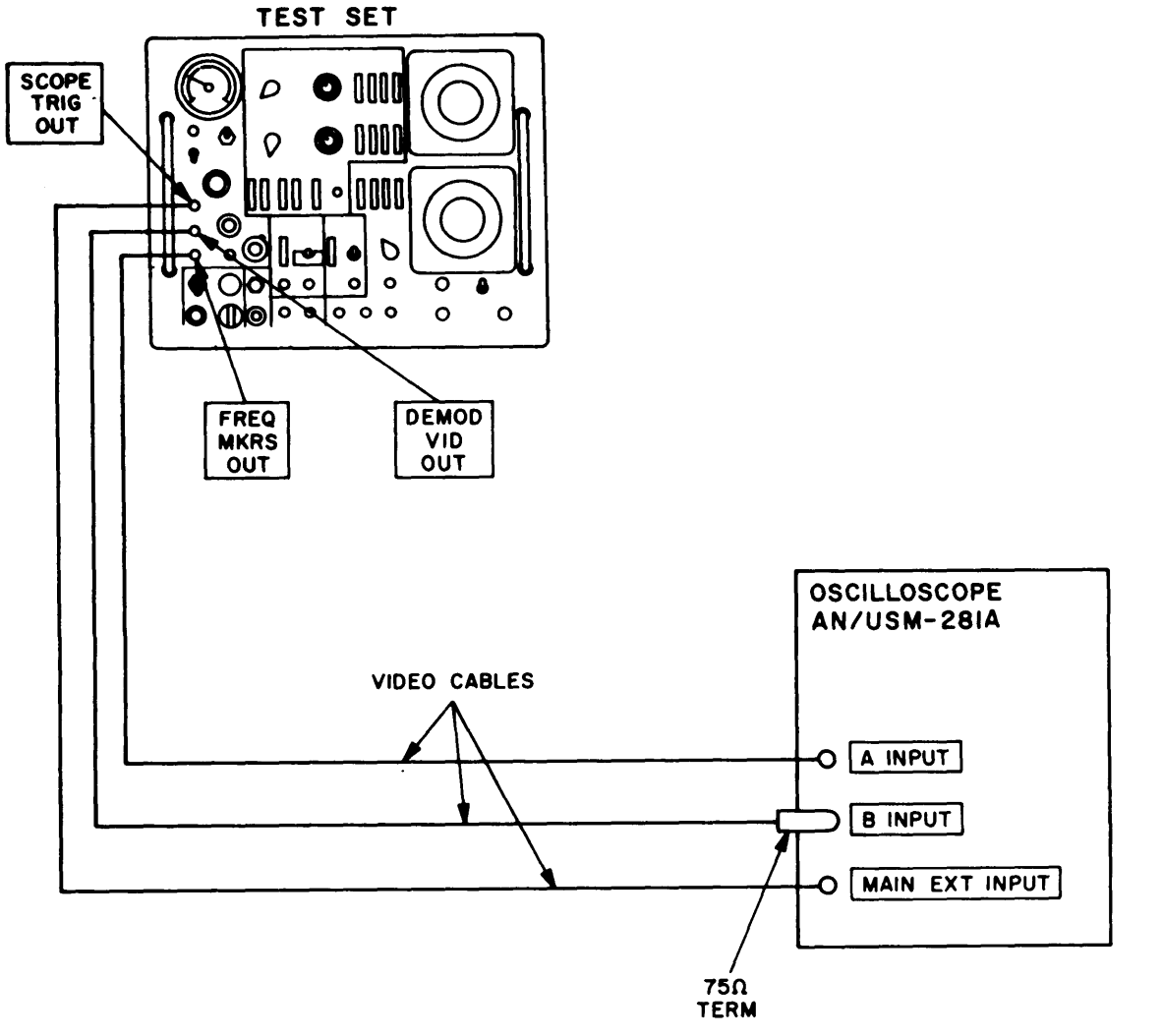


Figure 3–24. BIT frequency se(f test setup

Table 3–17 Delayed Rf Sweep Trigger Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure ***3–25.*** Set up frequency counter, paragraph 3–4e and as follows: B TRIGGER VOLTS switch: +2.	Set up test set, paragraph ***3–4b*** except: SIG GEN FUNCTION switch: SWP ±5 MHZ. PRT SEL (μ SEC) switches: 9999.	Observe frequency counter indication (delay from radar trigger to scope trigger).	Delay is equal to or less than 10 μsec.

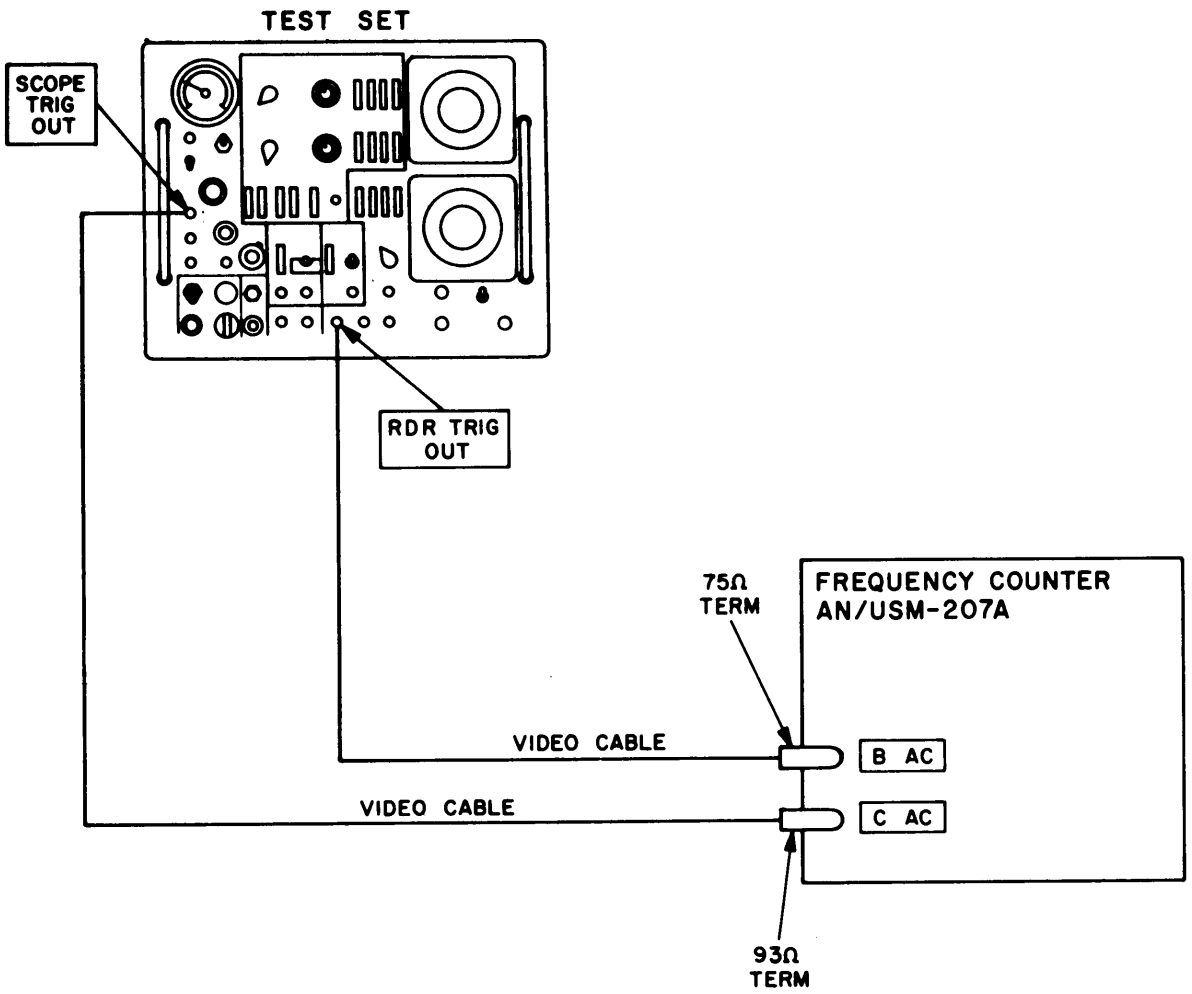


Figure 3-25 Delayed rf sweep trigger and sweep flequency mode PRF countdown test setup.

Table 3-17. Delayed Rf Sweep Trigger Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (Cont.)	B MULTIPLIER switch: 3. C TRIGGER VOLTS switch: +2. C MULTIPLIER switch: 1. Mode selector switch: SEP. FUNCTION switch: TIME B → C. Time base switch: 10^{7}.			

Table 3–17 Delayed Rf Sweep Trigger Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
2		MEASUREMENT FREQ MEAS control: ccw.	Observe frequency counter indication (delay from radar trigger to scope trigger).	Delay is equal to or greater than 10,000 μsec.

Table 3– 18. Sweep Frequency Mode PRF Countdown Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–25. Set up frequency counter, paragraph 3–4e and as follows: SENSITIVITY switch: FREQ C. C TRIGGER VOLTS switch: +2. c MULTIPLIER switch: 1. Mode selector switch: SEP. FUNCTION switch: FREQ. Time base switch: 1.	Set up test set, paragraph *3–4b* except: SIG GEN FUNCTION switch: SWP ±5 MHZ.	Observe frequency counter indication.	Frequency is 640 to 960 Hz.
2		PRT SEL (μSEC) switches: 1000.	Observe frequency counter indication.	Frequency is 400 to 600 Hz.
3		PRT SEL (μSEC) switches: 9999.	Observe frequency counter indication.	Frequency is 80 to 120 Hz.
4		SIG GEN FUNCTION switch: SWP ±15 MHZ.	Observe frequency counter indication.	Frequency is 80 to 120 Hz.
5		PRT SEL (μSEC) switches: 2000.	Observe frequency counter indication.	Frequency is 200 to 300 Hz.
6		PRT SEL (μSEC) switches: *0500.*	Observe frequency counter indication.	Frequency is *360* to 540 Hz.

Table 3-19. Decode Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–26.	Set up test set, paragraph *3–4b* except: SIF CHAL VID	Observe oscilloscope.	Reply pulse train present.

Table 3–19. Decode Functional Test-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (cont.)	Set up oscilloscope, paragraph 3–4c except: MAIN TIME/DIV switch: 50 µSEC.	SIF MODE SEL switch: 1.		
2		TRIG SEL DCD MODE SEL switch: 1.	*a.* Observe oscilloscope and test set REPLIES REPLY INHIB indicator. *b.* Press and hold test set BIT (MOM) switch.	*a.* Reply disappears and REPLIES REPLY INHIB indicator lights. *b.* Reply pulse train reappears and REPLIES REPLY INHIB indicator extinguishes.
3		SIF CHAL VID SIF MODE SEL switch: 2.	*a.* Observe oscilloscope and test set REPLIES REPLY INHIB indicator. *b.* Press and hold test set BIT (MOM) switch.	*a.* Reply pulse train disappears and REPLIES REPLY INHIB indicator lights. *b.* Same as a, above.
4		TRIG SEL DCD MODE SEL switch: 2.	Press and hold test set BIT (MOM) switch.	Reply pulse train appears and REPLIES REPLY INHIB indicator extinguishes.
5		SIF CHAL VID SIF MODE SEL switch: 3/A.	*a.* Observe oscilloscope and test set REPLIES REPLY INHIB indicator. *b.* Press and hold test set BIT (MOM) switch.	*a.* Reply pulse train disappears and REPLIES REPLY INHIB indicator lights. *b.* Same as a, above.
6		TRIG SEL DCD MODE SEL switch: 3/A.	Press and hold test set BIT (MOM) switch.	Reply pulse train reappears and REPLIES REPLY INHIB indicator extinguishes.
7		SIF CHAL VID SIF MODE SEL switch: C.	*a.* Observe oscilloscope and test set REPLIES REPLY INHIB indicator. *b.* Press and hold test set BIT (MOM) switch.	*a.* Reply pulse train disappears and REPLIES REPLY INHIB indicator lights. *b.* Same as a, above.
8		TRIG SEL DCD MODE SEL switch: C.	Press and hold test set BIT (MOM) switch.	Reply pulse train reappears and REPLY INHIB indicator extinguishes.
9		SIF CHAL VID SIF MODE SEL switch: OFF. REPLIES MODULATION SEL switch: M4–3P.	Observe oscilloscope and test set REPLIES REPLY INHIB indicator.	Reply pulse train disappears and REPLIES REPLY INHIB indicator lights.
10		TRIG SEL DCD MODE SEL switch: 4.	Press and hold test set BIT (MOM) switch.	Three pulse signal reply appears and REPLIES REPLY INHIB indicator extinguishes.

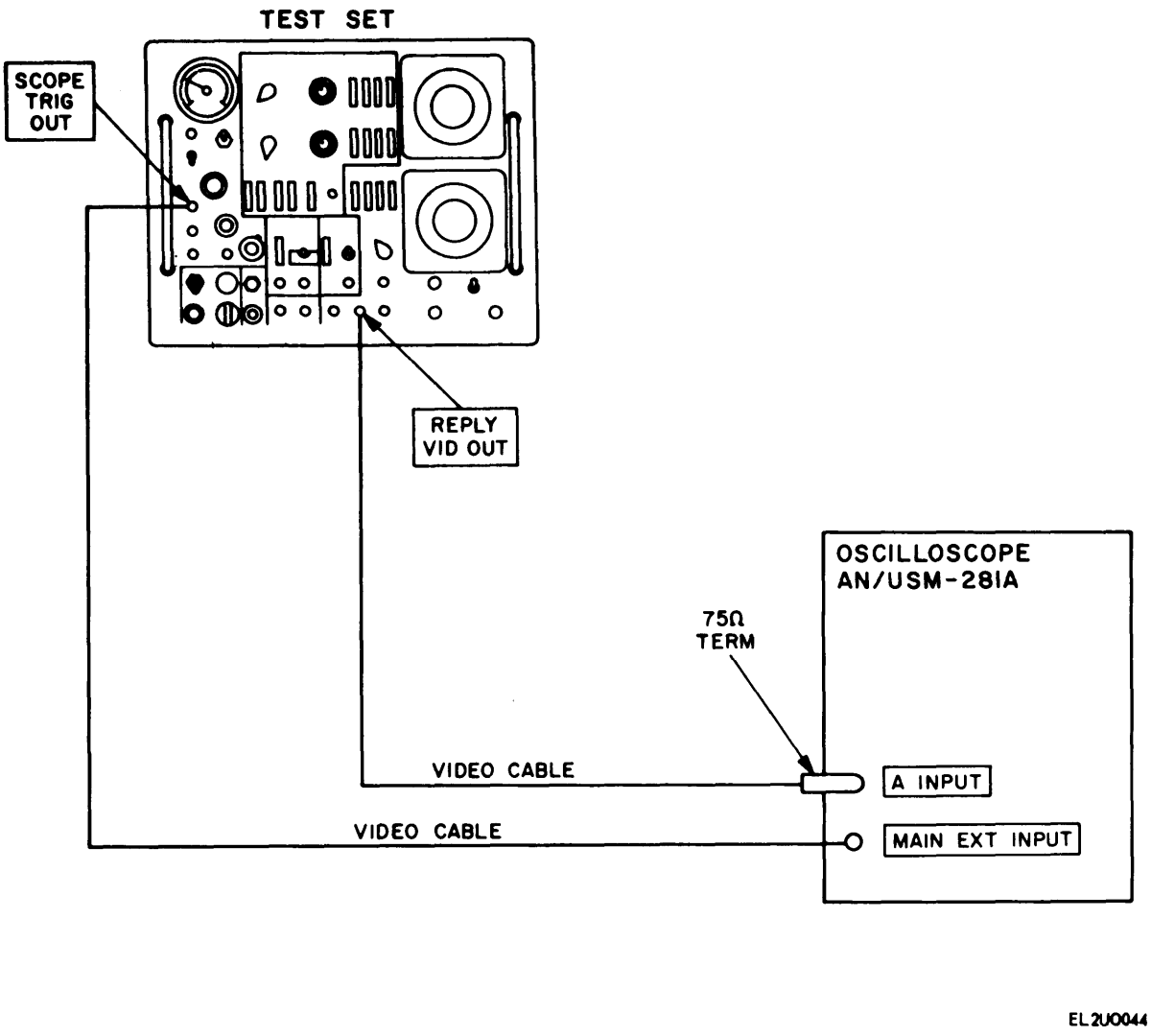


Figure 3-26. Decode test setup.

Table 3–20. SIF Challenge Video Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure *3–27*. Set up oscilloscope, paragraph 3–4c except as follows: MAIN TIME/DIV switch: 50 µSEC. DELAYED TIME/DIV switch: 1 µsec	Set up test set, paragraph *3–4b* except as follows: CHAL VID SIF MODE SEL switch: 1. SIF CHAL VID 5V/20V switch:5V.	Adjust oscilloscope DIV DELAY control to observe two SIF challenge pulses on A input and timing markers on B input.	Two pulses spaced 3.0 ±0.1 µsec.

Table 3-20. SIF Challenge Video Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (cont.)	SWEEP DISPLAY switch: DELAYED. DISPLAY switch: ALT.			
2	Oscilloscope: DELAYED TIME/DIV switch: .2 µSEC.		Adjust oscilloscope DIV DELAY control to observe one challenge video pulse on A input.	*a.* Pulse amplitude is 5.0 ±*0.5V.* *b.* Pulse width is 0.80 ±0.05 µsec.
3	Oscilloscope: A INPUT VOLTS/DIV switch: 5.	SIF CHAL VID 5V/20V switch: 20V.	Observe pulse width of pulse on A input.	Pulse width is 0.80 ±0.05µsec.
4	Oscilloscope: DELAYED TIME/DIV switch: 1 µSEC		Adjust oscilloscope DIV DELAY control to observe two SIF challenge pulses on A input.	Pulse amplitude is 20.0 ±4.OV.
5		SIF CHAL VID SIF MODE SEL switch: 2.	Adjust oscilloscope DIV DELAY control to observe two SIF challenge pulses on A input and timing markers on B input.	Pulse spacing is 5.0 ±0.1µsec.
6		SIF CHAL VID SIF MODE SEL switch: 3/A.	Adjust oscilloscope DIV DELAY control to observe two SIF challenge pulses on A input and timing markers on B input.	Pulse spacing is 8.0 ±0.1µsec.
7	Oscilloscope: DELAYED TIME/DIV switch: 5µSEC.	SIF CHAL VID SIF MODE SEL switch: C.	Adjust oscilloscope DIV DELAY control to observe two SIF challenge pulses on A input and timing markers on B input.	Pulse spacing is 21.0 ±0.1µsec.
8	Oscilloscope: DELAYED TIME/DIV switch: 1 µSEC.		*a.* Remove cable from MEASUREMENT TIMING MKRS OUT jack and connect to REPLY VID OUT jack.	*a.* None.
			b. Adjust oscilloscope DIV DELAY control to observe challenge P3 pulse (second pulse) on A input and first reply pulse (Fl) on B INPUT.	*b.* Delay is *4.0±0.2µsec.*

Table 3–21, Pulse Repetition Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure *3–28.* Set up frequency counter, paragraph 3–4e and as follows:	Set up test set as described in paragraph *3–4b.*	Observe frequency counter indication.	Period is 500 ±0.2 µsec.

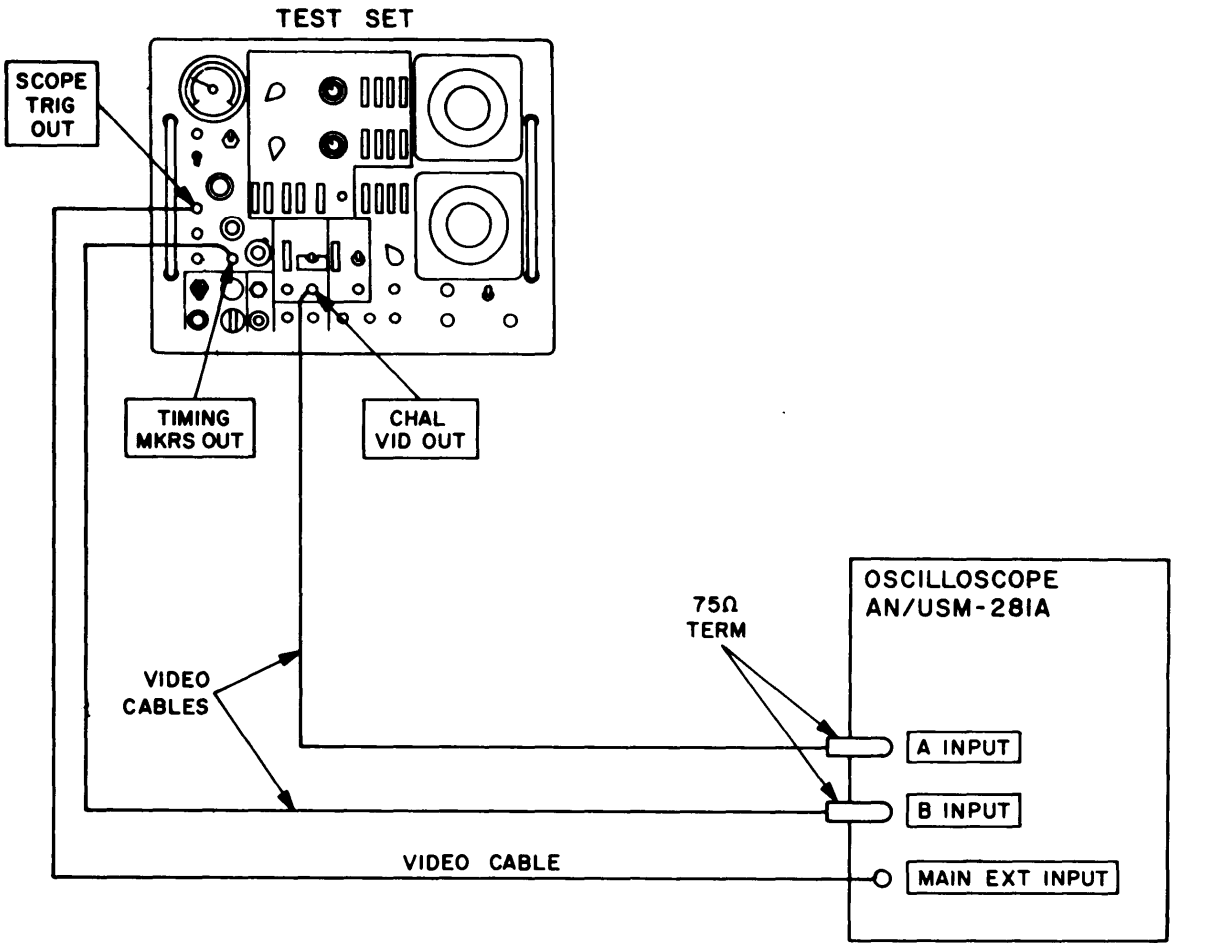


Figure 3–27. SIF challenge video test setup,

Table 3–21. Pulse Repetition Functional Test-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (cont.)	B and C SLOPE switches: +. B and C MULTIPLIER switches: 3. B and C VOLTS switches: +2. COM/SEP switch: COM. FUNCTION switch: TIME B→C. Time Base switch: 107.			

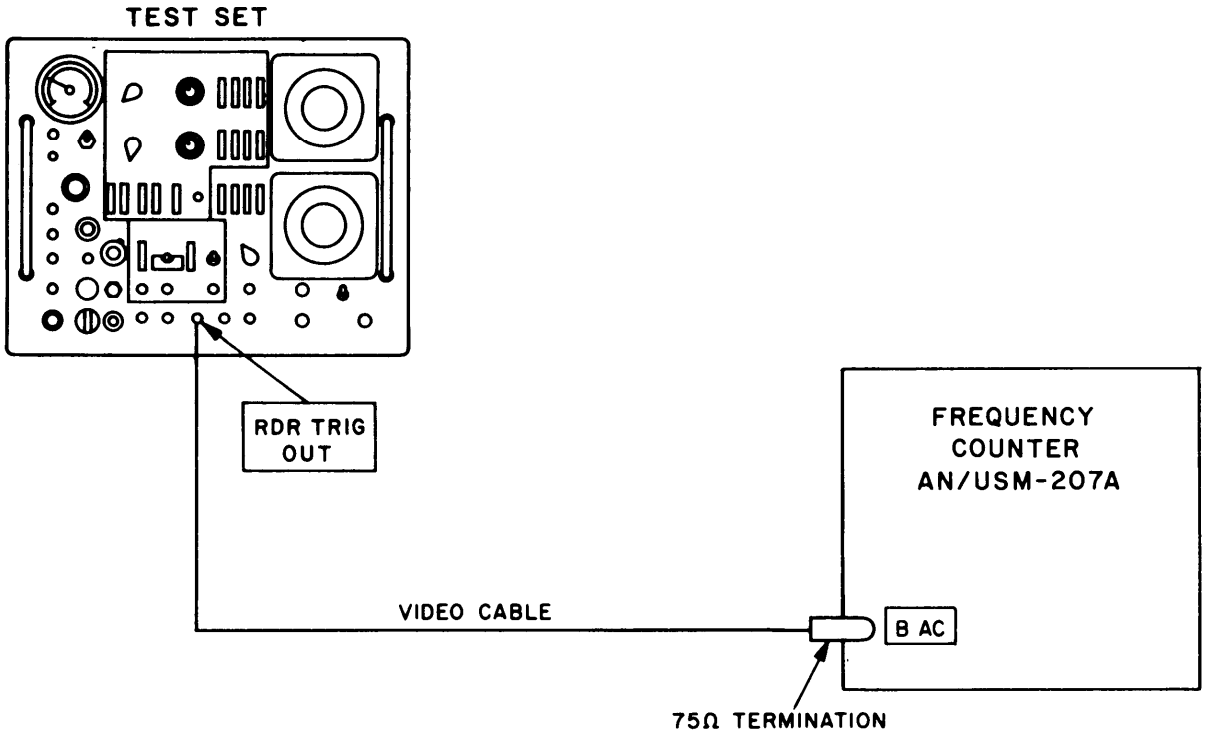


Figure 3-28. Pulse repetition test setup.

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Table 3-21. Pulse Repetitional Functional Test-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
2		PRT SEL (µSEC) switches: 0511.	Observe frequency counter indication.	Period is 511 ±0.2µsec.
3		PRT SEL (µSEC) switches: 0522.	Observe frequency counter indication.	Period is 522 ±0.2µsec.
4		PRT SEL (µSEC) switches: 0533.	Observe frequency counter indication.	Period is 533 ±0.2µsec.
5		PRT SEL (µSEC) switches: 0544.	Observe frequency counter indication.	Period is 544 ±0.2µsec.
6		PRT SEL (µSEC) switches: 0555.	Observe frequency counter indication.	Period is 555 ±0.2µsec.
7		PRT SEL (µSEC) switches: 0566.	Observe frequency counter indication.	Period is 566 ±0.2µsec.
8		PRT SEL (µSEC) switches: 0577.	Observe frequency counter indication.	Period is 577 ±0.2µsec.
9		PRT SEL (µSEC) switches: 0588.	Observe frequency counter indication.	Period is 588 ±0.2µsec.
10		PRT SEL (µSEC) switches: 0599.	Observe frequency counter indication.	Period is 599 ±0.2µsec.

Tab/e 3–21. Pulse Repetition Functional Test—Continued

step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
11		PRT SEL (µSEC) switches: 1000.	Observe frequency counter indication.	Period is 1000 ±0.2µsec.
12		PRT SEL (µSEC) switches: 1100.	Observe frequency counter indication.	Period is 1100 ±0.2µsec.
13		PRT SEL (µSEC) switches: 2200.	Observe frequency counter indication.	Period is 2200 ±0.2µsec.
14		PRT SEL (µSEC) switches: 3300.	Observe frequency counter indication.	Period is 33OO±0.3 µsec.
15		PRT SEL (µSEC) switches: 4400.	Observe frequency counter indication.	Period is 4400 ±0.4µsec.
16		PRT SEL (µSEC) switches: 5500.	Observe frequency counter indication.	Period is 5500 ±0.6µsec.
17		PRT SEL (µSEC) switches: 6600.	Observe frequency counter indication.	Period is 660O±0.7µsec.
18		PRT SEL (µSEC) switches: 7700.	Observe frequency counter indication.	Period is 7700 ±0.8µsec.
19		PRT SEL (µ SEC) switches: 8800.	Observe frequency counter indication.	Period is 8800 ±0.9µsec.
20		PRT SEL (µSEC) switches: 9900.	Observe frequency counter indication.	Period is 9900±0.9µsec.

Table 3–2.2. *Pulse Repetition Measurement Functional Test*

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–29. Set up oscilloscope, paragraph 3–4c except as follows: A VOLT/DIV switch: .5. MAIN TIME/DIV switch: 10 µSEC. DELAYED TIME/ DIV switch: .1 µSEC. Set up frequency counter, paragraph 3–4e and as follows: SENSITIVITY switch: FREQ C. c MULTIPLIER switch: .3. C TRIGGER VOLTS control: O.	Set up test set as described in paragraph 3–6, except: MEASUREMENT FUNCTION SEL switch: PRF EXT. MEASUREMENT PRF RANGE switch: X1OO.	Observe test set MEASUREMENT meter prf indication,	MEASUREMENT meter indicates 101 ±5% or ±5° of meter, whichever is larger. NOTE Steps 1 through 7 are calculated by multiplying MEASUREMENT PRF RANGE setting by MEASUREMENT meter reading.

Table 3–22. Pulse Repetition Measurmement Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (cont.)	COM/SEP switch: SEP. FUNCTION switch: FREQ. Time base switch: 1. Set up pulse generator, paragraph *3–4f* and pulse with following characteristics: Sync Selector: INT A. Pulse rate: 101 Hz (read on frequency counter). Pulse width: 0.50 ‘ µsec. Pulse amplitude: +3V. Pulse rise time: 0.1 µsec.			
2		MEASUREMENT PRF RANGE switch: Xl0.	Adjust pulse generator prf until frequency counter indicates 90 Hz. Observe test set MEASUREMENT meter indication.	MEASUREMENT meter indicates 90 Hz ±5% or ±5° of meter, whichever is greater.
3	Set pulse generator sync switch to INT B.	MEASUREMENT PRF RANGE switch: X1OO.	Adjust pulse generator prf until frequency counter indicates 1000 Hz. Observe MEASUREMENT meter indication.	MEASUREMENT meter indicates 1000 Hz ±5% or±5° of meter, whichever is greater.
4		MEASUREMENT PRF RANGE switch: XIK.	Observe MEASUREMENT meter indication.	MEASUREMENT meter indicates 1000 ±5% or ±5° of meter whichever is greater.
5	Set pulse generator SYNC switch to INT C.		Adjust pulse generator prf until frequency counter indicates 2000 Hz. Observe MEASUREMENT meter indication.	MEASUREMENT meter indicates 2000 Hz ±5% or ±5° of meter, whichever is greater.
6	Set frequency counter C MULTIPLIER switch to 3. Set up pulse generator for pulse with the following characteristics: Pulse rate: 101 Hz. Pulse width: 1.5 µsec. Pulse amplitude: +20V.	MEASUREMENT EXT VID IN 75 Ω/2κ Ω switch: 2κΩ Repeat steps 1 through 5.	Repeat steps 1 through 5.	Same as steps 1 through 5.
7	Repeat steps 1 through 6 with pulse generator set for -3 v and -20 v output.	Repeat steps 1 through 6.	Repeat steps 1 through 6,	Same as steps 1 through 6.

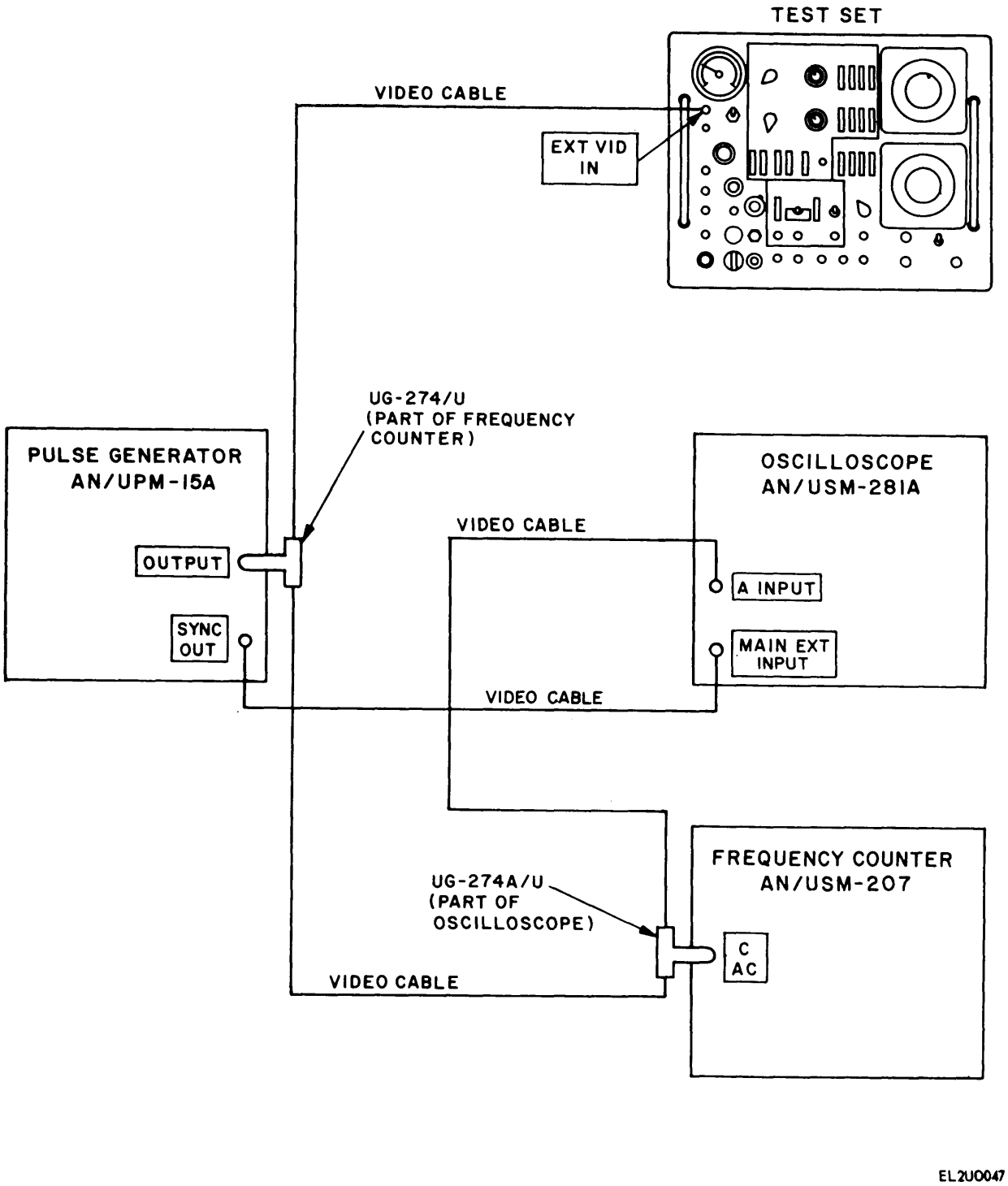

Figure 3–29. PuIse repetitioion measurement test setup.

Table 3–.23. External Trigger Input Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–30. Set up frequency counter, paragraph 3 –4e and as follows: FUNCTION switch: TIME B→C. Time base switch: 1 0". COM/SEP switch: COM. B and C MULTIPLIER switches: 3. B and C TRIGGER VOLTS switches: 0. B and C SLOPE switches: +. Set pulse generator per paragraph *3–4f* with pulse output as follows: Amplitude: +5 volts. Pulse width: 5.0 µsec. Repetition Time: 500 µsec. Set up oscilloscope as described in paragraph 3–4a except as follows: 4 A VOLTS/DIV switch: 2. MAIN TIME/DIV switch: 2 µSEC. DELAYED TIME/DIV switch: .5 @EC. EXT ÷ 10/EXT/INT/LINE switch: EXT.	Set up test set as described in paragraph *3–4b* except as follows: TRIG SEL switch: EXT.	a. Adjust pulse generator PULSE POSITION control until oscilloscope display is centered. *b.* Observe amplitude of pulse on A INPUT. *c.* Observe pulse width on A INPUT. *d.* Using rise time measurement procedure described in TM 11 –6625– 1703–15, measure pulse rise time. *e.* Using procedure in *d*, above, measure pulse fall time.	*a.* None. *b.* Pulse amplitude is 9 to 11 volts. *c.* Pulse width is 2 to 4 µsec. *d.* Pulse rise time is less than 0.1 µsec. *e.* Pulse fall time is less than 0.2 µsec.
2	Set oscilloscope DISPLAY switch to ALT.		Observe pulse spacing between pulses on A and B INPUTS.	Pulse spacing is less than 0.30 µsec.
3	Adjust pulse generator pulse width to 0.5 µsec.		Observe pulse spacing between pulses on A and B INPUTS.	Pulse spacing is less than 0.30 µsec.
4			a. Remove video cable from oscilloscope B INPUT jack and connect terminated video cable from test set MEASUREMENT SCOPE TRIG OUT jack to oscilloscope B INPUT. *b.* Measure spacing between pulses on A and B INPUT.	a. None.

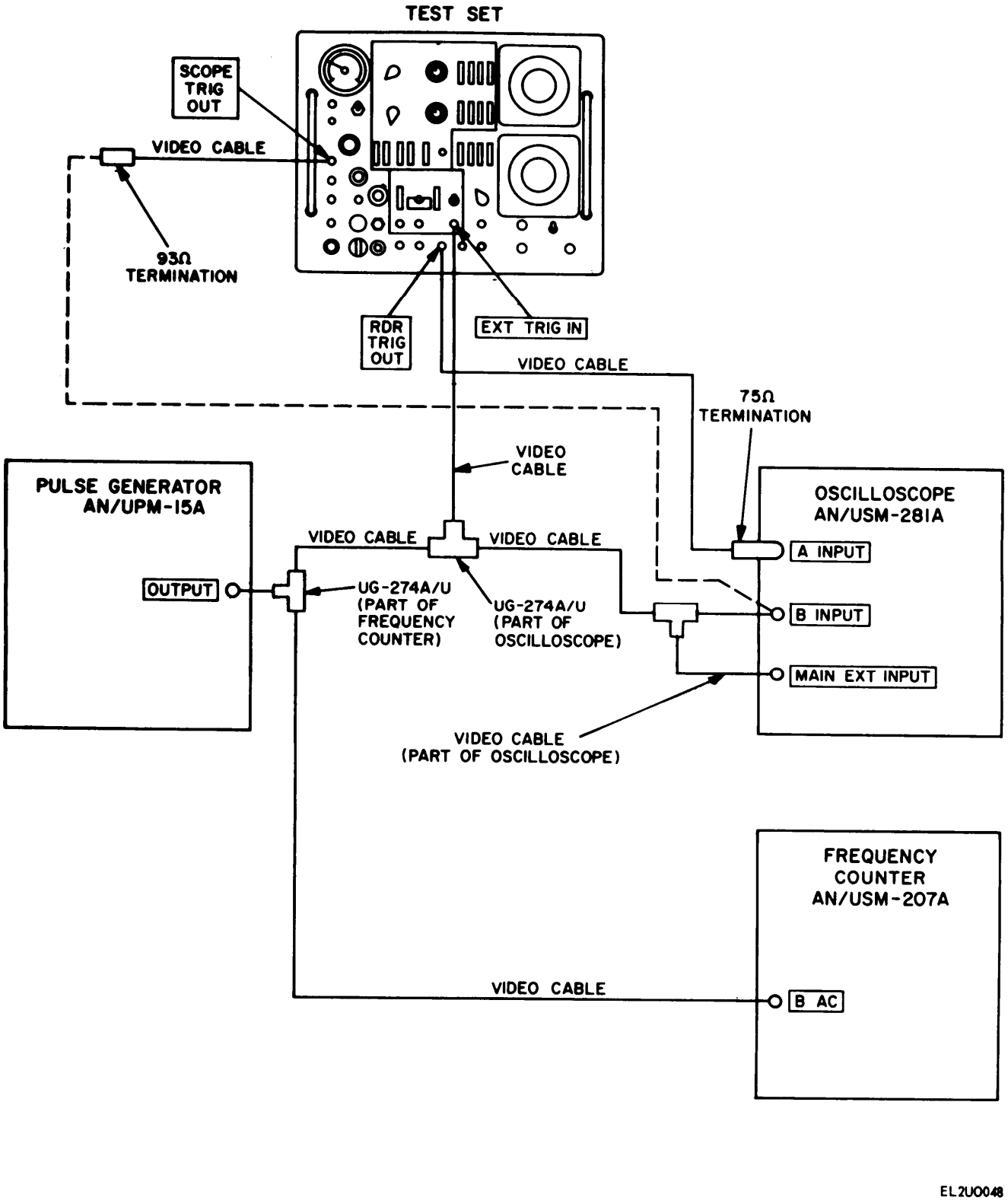

figure 3-30. External trigger test setup.

Table 3–23. External Trigger Input Functional Test—Continued

Step No.	Control settings: Test equipment	Control settings: Test set	Test procedure	Performance standard
4 (cont.)			c. Measure B INPUT pulse amplitude.	c. Pulse amplitude is 5.0 ±1 volt.
5	Pulse generator POLARITY switch: NEG. Frequency counter: B and C SLOPE switches: -. B and C TRIGGER switches: -2.		Adjust pulse generator for a frequency counter indication of 500 µsec. Repeat steps 1 through 4.	Same as steps 1 through 4.

Table 3–24. Range Delay Functional Test

Step No.	Control settings: Test equipment	Control settings: Test set	Test procedure	Performance standard
1	Connect test set as shown in figure 3–31. Set up oscilloscope, paragraph 3–4c except DISPLAY switch ALT A VOLT/DIV switch: 2. Set up frequency counter, paragraph 3–4e and as follows: SENSITIVITY switch: .lV. Time base switch: 10^7. Function switch TIME B →C. B and C SLOPE switches: +. B MULTIPLIER switch: 3. B TRIGGER VOLTS control: +2. C MULTIPLIER switch: 3. C TRIGGER VOLTS control: +2, COM/SEP switch: SEP.	Set up test set, paragraph *3–4b* except, set controls as follows: PRT SEL (µSEC) switches: 9999.	Observe frequency counter indication.	Frequency counter indicates 434.0 ±0.7 µsec. NOTE 434 µsec is a nominal delay delay and may be adjusted over the range of 360 µsec to 438 µsec (with the REPLIES RANGE DELAY SEL (µSEC) switches set for 0001). The deviation from nominal is determined by the specific system parameters of the Interrogator system under test.
2		REPLIES MODULATION SEL switch: M4–3P.	Observe frequency counter indication.	Frequency counter indicates 449.0 ±0.7 µsec. NOTE 449 µsec is a *nominal* delay and is dependent upon the delay setting of the mode 4 internal reference of 14.5 µsec.

Table 3–24. Range Delay Functional Test—Continued

step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
2 (cont.)				The mode 4 internal reference is adjustable over the range of 4 µsec to 34 µsec after the radar trigger by means of switches lA1S1, 1A1S2, and 1A1S3. The deviation from nominal is determined by specific system parameters of the interrogator system under test. The coupler measurement of step 2 indicates the nominal Mode 4 internal reference delay (14.5 µsec) plus 434.5 µsec plus the REPLIES RANGE DELAY SEL (µSEC) switches (0001) -1 = *449 µsec.*
3		REPLIES MODULATION SEL switch: SIF.		**NOTE** In steps 4 thru 14, the frequency counter indicates the RANGE DELAY SEL (µSEC) switch settings plus the internal delay (set to *434 µsec)* minus 1 µsec.
4		REPLIES RANGE DELAY SEL (µSEC) switches: 0111.	Observe frequency counter indication.	Frequency counter indicates 544.0 ±0.7 µsec.
5		REPLIES RANGE DELAY SEL (µ SEC) switches: 0222.	Observe frequency counter indication.	Frequency counter indicates 655.0 ± 0.7 µsec.
6		REPLIES RANGE DELAY SEL (µSEC) switches: 0333.	Observe frequency counter indication.	Frequency counter indicates 766.0 ±0.7 µsec.
7		REPLIES RANGE DELAY SEL (µSEC) switches: *0444.*	Observe frequency counter indication.	Frequency counter indicates 877.0 ±0.7 µsec.
8		REPLIES RANGE DELAY SEL 0555.	Observe frequency counter indication.	Frequency counter indicates 988.0 ±0.7 µsec.
9		REPLIES RANGE DELAY SEL (µSEC) switches: 0666.	Observe frequency counter indication.	Frequency counter indicates 1099.0 ± 1.1 µsec.
10		REPLIES RANGE DELAY SEL (µSEC) switches: 0777.	Observe frequency counter indication.	Frequency counter indicates 1210.0 ±1.1 µsec.
11		REPLIES RANGE DELAY SEL (µSEC) switches: 0888.	Observe frequency counter indication.	Frequency counter indicates 1321.0 ±1.1 µsec.

Table 3–24. Range Delay Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
12		REPLIES RANGE DELAY SEL (µSEC) switches: *0999.*	Observe frequency counter indication.	Frequency counter indicates 1432.0 ±1.1 µsec.
13		REPLIES RANGE DELAY SEL (µEC) switches: 1999.	Observe frequency counter indication.	Frequency counter indicates 2432.0 ±1.1 µsec
14		REPLIES RANGE DELAY SEL (µSEC) switches: 2999.	Observe frequency counter indication.	Frequency counter indicates 3432.0 ±1.1 µsec.
15	Set oscilloscope MAIN TIME/ DIV switch to .5 MSEC.	PRT SEL (µSEC) switches: 3400.	Observe REPLY INHIB indicator and oscilloscope.	REPLY INHIB indicator lights and oscilloscope B INPUT are inhibited.
16		PRT SEL (µSEC) switches: 3600.	Observe REPLY INHIB indicator and oscilloscope.	REPLY INHIB indicator extinguishes and pulses on oscilloscope B INPUT are displayed.

Table 3–25. SIF Reply and Substitute Pulse Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test set up as shown in figure 3–32. Set up oscilloscope, paragraph 3–4c. MAIN TIME/ DIV switch: 50 µSEC. DELAYED TIME/ DIV switch: 5 µSEC.	Set up test set, paragraph *3–46.*	*a.* Observe number of pulses on A INPUT. *b.* Measure pulse amplitude.	a. Oscilloscope displays 8-pulse reply train. *b,* Pulse amplitude is 5±0.5 volts.
2	Oscilloscope: DELAYED TIME/DIV switch: .1 µSEC. DISPLAY switch: ALT.		Using the oscilloscope CRT graticule, measure and record the distance between the 10'% and 90% amplitude points.	Pulse rise time is less than 0.1 µsec. Pulse fall time is less than 0.2 µsec.
3		REPLIES REPLY WIDTH SELECT switch: 0.15.	Observe pulse width.	Pulse width is 0.15 ±0.05 µsec.
4		REPLIES REPLY WIDTH SELECT switch: 0.45.	Measure pulse width.	Puke width is 0.45 ±0.05 µsec.

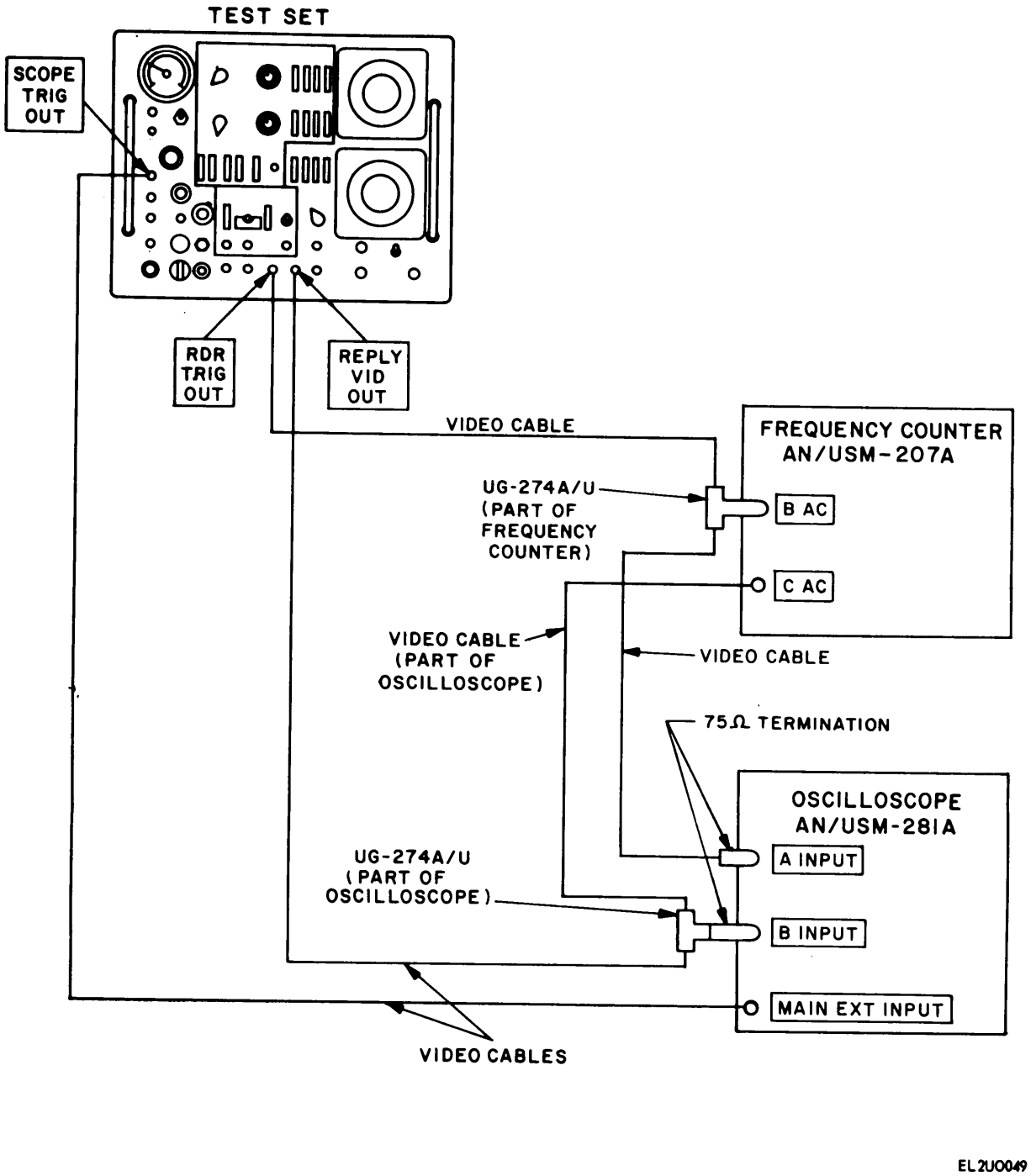

Figure 3-31. Range deduy test setup.

Tabe 3-25. SIF Reply and Substitute Pulse Functinal Test-Continued

step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
5		REPLIES REPLY WIDTH SELECT switch: 0.50.	Measure pulse width.	Pulse width is 0.50 ±0.05µsec.
6		REPLIES REPLY WIDTH SELECT switch: 0.90.	Measure pulse width.	Pulse width is 0.90 ±0.05 µsec.
7	oscilloscope: DELAYED TIME/DIV switch:.5 µEC.	REPLIES REPLY WIDTH SELECT switch: VARY	Adjusts REPLIES REPLY WIDTH VARY control throughout its range.	Pulse width can be varied from less than 0.15 to more than 1.50 µsec.
8	oscilloscope: DELAYED TIME/DIV switch: .1 µSEC.	REPLIES REPLY WIDTH SELECT switch: 0.45. SIF REPLY CODE switches: 0010.	a. Adjust oscilloscope DIV DELAY control to align F1 pulse on A INPUT to center graticule for reference. Note position with respect to TIMING markers on B INPUT. *b.* Adjust oscilloscope DIV DELAY control to align Cl pulse to center graticule (reference) while counting markers. c. Use timing markers to interpolate pulse spacing from F1 pulse to Cl pulse.	*b.* None.
9		SIF REPLY CODE switches: 1000.	Using procedure in step 8, determine spacing between F1 and Al pulses.	Pulse spacing is 2.90 ±0.02 µsec.
10		S1F REPLY CODE switches: 0020.	Using procedure in step 8, determine spacing between F1 and C2 pulses.	Pulse spacing is 4.35 ±0.02 µsec.
11		S1F REPLY CODE switches: 2000.	Using procedure in step 8, determine spacing between F1 and A2 pulses.	Pulse spacing is 5.80 ±0.02 µsec.
12		S1F REPLY CODE switches: 0040.	Using procedure in step 8, determine spacing between F1 and C4 pulses.	Pulse spacing is 7.25 ±0.02 µsec.
13		SIF REPLY CODE switches: 4000.	Using procedure in step 8, determine spacing between F1 and A4 pulses.	Pulse spacing is.8.70 ±0.02 µsec.
14		SIF REPLY CODE switches: 0100.	Using procedure in step 8, determine spacing between F1 and B1 pulses.	Pulse spacing is 11.60 ±0.02 µsec.
15		SIF REPLY CODE switches: 0001.	Using procedure in step 8, determine spacing between F1 and D1 pulses.	Pulse spacing is 13.05 ±0.02 µsec.
16		SIF REPLY CODE switches: 0200.	Using procedure in step 8, determine spacing between F1 and B2 pulses.	Pulse spacing is 14.50 ±0.02 µsec.
17		SIF REPLY CODE switches: 0002.	Using procedure in step 8, determine spacing between F1 and D2 pulses.	Pulse spacing is 15.95 ±0.02 µsec.
18		SIF REPLY CODE switches: 0400.	Using procedure in step 8, determine spacing between F1 and B4 pulses.	Pulse spacing is 17.40 ±0.02 µsec.
19		SIF REPLY CODE switches: 0004.	Using procedure in step 8, determine spacing between F1 and D5 pulses.	Pulse spacing is 18.85 ±0.02 µsec.

Table 3–25. SIF Reply and Substitute Pulse Functional Test-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
20		SIF REPLY CODE switches: 0000.	Using procedure in step 8, determine spacing between F1 and F2 pulses.	Pulse spacing is 20.30 ±0.02 µsec.
21		REPLIES SUB PULSE SEL switch: Cl. SIF REPLY CODE switches: 0010.	Repeat step 8 to determine spacing between F1 and Cl pulses.	Pulse spacing is 1.45 ±0.02 µsec.
22		REPLIES SUB PULSE POS SELECT switch: -0.50.	Using procedure in step 8, measure pulse spacing between F1 and Cl pulses.	Pulse spacing is 0.95 ±0.02 µsec.
23		REPLIES SUB PULSE POS SELECT switch: -0.35.	Using procedure in step 8, measure pulse spacing between F1 and Cl pulses.	Pulse spacing is 1.10 ±0.02 µsec.
24		REPLIES SUB PULSE POS SELECT switch: -0.25.	Using procedure in step 8, measure pulse spacing between F1 and Cl pulses.	Pulse spacing is 1.20 ±0.02 µsec.
25		REPLIES SUB PULSE POS SELECT switch: -0.15.	Using procedure in step 8, measure pulse spacing between F1 and Cl pulses.	Pulse spacing is 1.30 ±0.02 µsec.
26		REPLIES SUB PULSE POS SELECT switch: +0.15.	Using procedure in step 8, measure pulse spacing between F1 and Cl pulses.	Pulse spacing is 1.60 ±0.02 µsec.
27		REPLIES SUB PULSE POS SELECT switch: +0.25.	Using procedure in step 8, measure pulse spacing between F1 and Cl pulses.	Pulse spacing is 1.70 ±0.02 µsec.
28		REPLIES SUB PULSE POS SELECT switch: +0.35.	Using procedure in step 8, measure pulse spacing between F1 and Cl pulses.	Pulse spacing is 1.80 ±0.02 µsec.
29		REPLIES SUB PULSE POS SELECT switch: +0.50.	Using procedure in step 8, measure pulse spacing between F1 and Cl pulses.	Pulse spacing is 1.95 ±0.02 µsec.
30		REPLIES SUB PULSE POS SELECT switch: VARY. REPLIES SIF REPLY CODE switches: 2000. REPLIES SUB PULSE SEL switch: A2.	Adjust REPLIES SUB PULSE POS VARY control throughout its range and using procedure in step 8, determine pulse spacing at minimum and maximum points between F1 and Cl pulses.	Pulse spacing varies from less than 5.0O to more than 6.60 µsec.

Table 3-25. SIF Reply and Substitute Pulse Functional Test-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
31	Oscilloscope: DELAY TIME/ DIV switch: 2 µ SEC.	REPLIES SUB PULSE POS SELECT switch: +0.25. SIF REPLY CODE switches: 7777. SIF REPLIES SUB PULSE SEL switch: OFF.	*a.* While observing Cl pulse, set REPLIES SUB PULSE SEL switch to Cl. *b.* While observing Al pulse, set REPLIES SUB PULSE SEL switch to Al. *c.* While observing C2 pulse, set REPLIES SUB PULSE SEL switch to C2. *d.* While observing A2 pulse, set REPLIES SUB PULSE SEL switch to A2. *e.* While observing C4 pulse, set REPLIES SUB PULSE SEL switch to C4. *f.* While observing A4 pulse, set REPLIES SUB PULSE SEL switch to A4. *g.* While observing B1 pulse, set REPLIES SUB PULSE SEL switch to B1. *h.* While observing D1 pulse, set REPLIES SUB PULSE SEL switch to D1. *i.* While observing B2 pulse, set REPLIES SUB PULSE SEL switch to B2. j. While observing D2 pulse, set REPLIES SUB PULSE SEL switch to D2. *k.* While observing B4 pulse, set REPLIES SUB PULSE SEL switch to B4. *1.* While observing D4 pulse, set REPLIES SUB PULSE SEL switch to D4. *m.* While observing BRKT–2 pulse, set REPLIES SUB PULSE SEL switch to BRKT–2.	*a.* Cl pulse moves. *b.* Al pulse moves (Cl returns to normal position). c. C2 pulse moves (Al returns to normal position). *d.* A2 pulse moves (C2 returns to normal position). e. C4 pulse moves (A2 returns to normal position). *f.* A4 pulse moves (C4 returns to normal position). *g.* B1 pulse moves (A4 returns to normal position). *h.* D1 pulse moves (Bl returns to normal position). *i.* B2 pulse moves (D1 returns to normal position). *j.* D2 pulse moves (B2 returns to normal position). *k* B4 pulse moves (D2 returns to normal position). *l.* D4 pulse moves (B4 returns to normal position). *m.* BRKT–2 (F2) moves and D4 returns to normal position.
32	Oscilloscope: DELAYED TIME/ DIV switch: 5µSEC.	REPLIES MODULATION SEI, switch: I/P Ml. REPLIES SUB PULSE POS SELECT switch: O.	Observe pulse trains.	Two pulse trains appear.
33		REPLIES MODULATION SEL switch: I/P M2/3. PRT SEL (µSEC) switches: 0600.	Observe pulse train.	SIF reply train followed by single (SPI) pulse appears.
34	oscilloscope: MAIN TIME/ DIV switch: .1 MSEC. DELAYED TIME/DIV switch: 10 µSEC.	REPLIES MODULATION SEL switch: EMERG.	Adjust oscilloscope DIV DELAY control to observe pulse train.	SIF reply train followed by three sets of bracket (BRKT– 1 and BRKT–2) pulses.

Table 3-25. SIF Reply and Substitute Pulse Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
35		REPLIES MODULATION SEL switch: GARBLE.	Observe pulse train.	SIF reply train followed by one pulse spaced *20.3 μec* after BRKT–2 pulse.

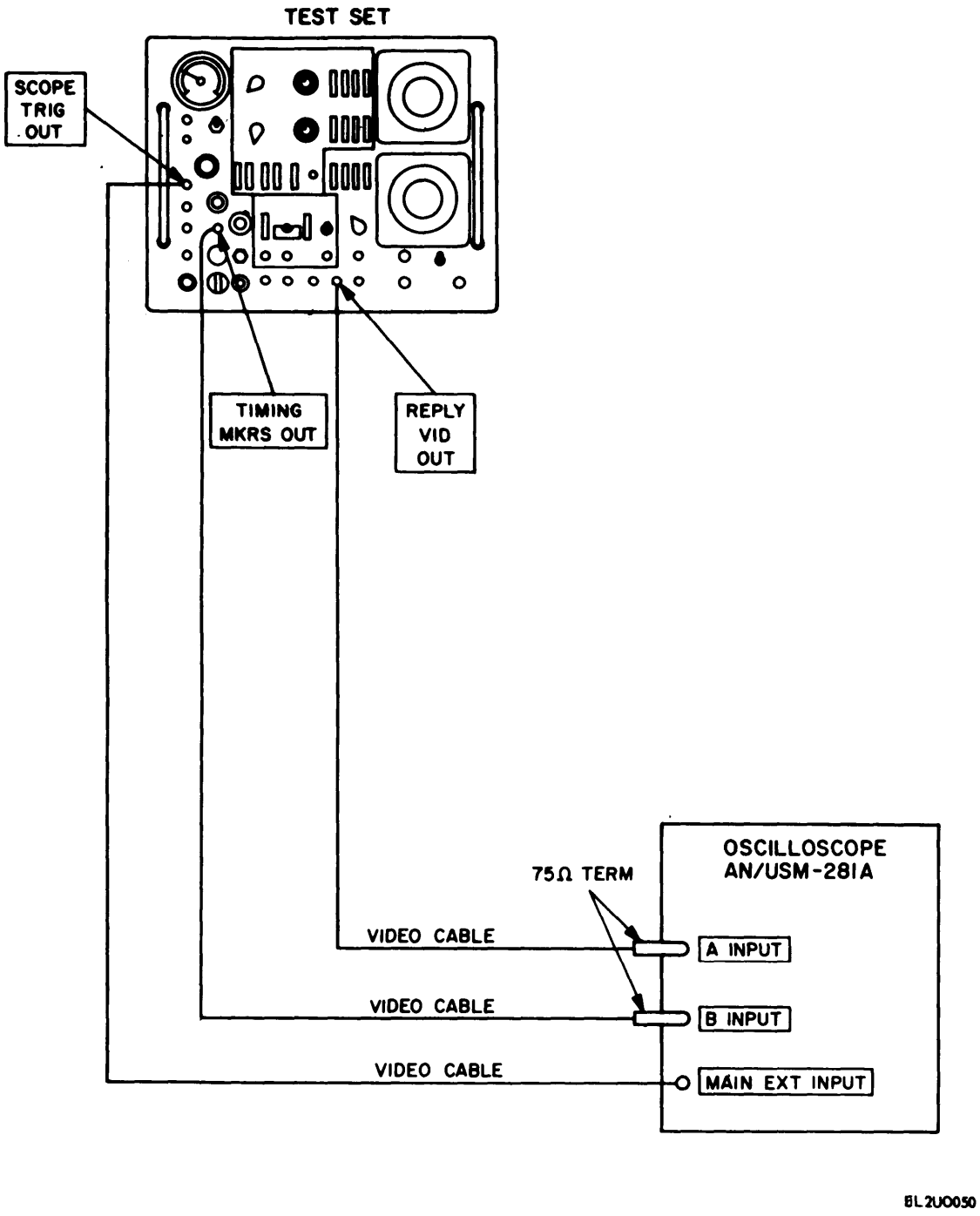

Figure 3–32. SIF reply and substitute puLse spacing, and mode 4 reply setup

Table 3-26. Mode 4 Reply Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3-32. Set up oscilloscope, paragraph 3–4c except as follows: DISPLAY switch: ALT. MAIN TIME/DIV switch: 50 µSEC. DELAYED TIME/DIV switch:.5 µSEC. Sweep display switch: DELAYED.	Set up test set, paragraph *3–4b*, except as follows: REPLIES MODULATION SEL switch: M4–3P.	*a.* Adjust oscilloscope DIV DELAY control to center reply pulses on CRT display; observe pulses on A INPUT. *b.* Measure P1 to P2 and P2 to P3 pulse spacing. *c.* Measure pulse amplitude.	*a.* Reply consists of three pulses. *b.* Pulse spacing is 1.8 ±0.05 µsec. *c.* Pulse amplitude is 5.0 ±0.5 volts.
2		REPLIES SUB PULSE SEL switch: M4–P2. REPLIES SUB PULSE POS SELECT switch: +.25.	Observe second pulse.	Second pulse moves.
3		REPLIES SUB PULSE SEL switch: M4 – P3.	Observe third pulse.	Third pulse moves (second pulse returns to normal position).
4		REPLIES SUB PULSE SEL switch: OFF. REPLIES MODULATION SEL switch: M4–lP.	*a.* Observe pulse. *b.* Set oscilloscope DELAYED TIME/DIV switch to .1 @EC and sweep display switch to MAIN; using rise time measurement procedure outlined in TM 11–6625–1703–15, measure pulse rise time. *c.* Measure pulse fall time.	*a.* Only pulse in third puke position is present. *b.* Rise time is less than 0.10 µsec. *c.* Fall time is less than 0.20 µsec.
5	*A* VOLT/DIV switch: 1. 4 VOLT/WDIV vernier: CAL. DISPLAY switch: A. Sweep display switch: MAIN.	REPLIES M4 JAMMING switch: 1.	Observe waveform.	Three jamming pulses appear ahead of reply pulse. NOTE In steps 5 through 9 jamming pulses are counted down (baseline present) and the mode 4 one pulse reply is solid (no baseline).
6		REPLIES M4 JAMMING switch: 2.	Observe waveform.	Six jamming pulses appear ahead of reply pulse.
7		REPLIES M4 JAMMING switch: 3.	Observe waveform.	Nine jamming pulses appear ahead of reply pulse.

Table 3–26. Mode 4 Reply Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
8		REPLIES M4 JAMMING switch: 4.	Observe waveform.	Twelve jamming pulses appear ahead of reply pulse.
9		REPLIES M4 JAMMING switch: 5.	Observe waveform.	Fifteen jamming pulses appear ahead of reply pulse.

Table 3–27. Variable Gating Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–33. Set up counter as described in paragraph 3–4e, and as follows: SENSITIVITY switch: FREQ C. B MULTIPLIER switch: 3. B TRIGGER VOLTS switch: +2. C MULTIPLIER switch: 10. C TRIGGER VOLTS switch: +2. FUNCTION switch: PERIOD B x M 10^{3}. Time base switch: 10^{8}. DISPLAY control: midrange.	Set up test set per paragraph *3–4b*, except as follows: REPLIES MODULATION SEL switch: M4–l P.	Measure ratio of RDR TRIG signals to REPLY VID OUT signals by observing counter.	Ratio is 1.000 ±0.010.
2		REPLIES GATING PASS switches: 01. REPLIES GATING INHIB switches: 09,	Momentarily press frequency counter RESET switch. Observe frequency counter indication.	Frequency counter indication is 10.000±0.010.
3		REPLIES GATING PASS switches: *02*. REPLIES GATING INHIB switches: 08.	Momentarily press frequency counter RESET switch.	Frequency counter indication is 5.000±O.O1O.
4		REPLIES GATING PASS switches: *03*. REPLIES GATING INHIB switches: 07.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 3.333±0.010.
5		REPLIES GATING PASS switches: *04*. REPLIES GATING INHIB switches: 06.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 2.500±0.010.

Table 3-27. Variable Gating Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
6		REPLIES GATING PASS switches: 05. REPLIES GATING INHIB switches: 05.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 2.000 ±O.O1O.
7		REPLIES GATING PASS switches: 06. REPLIES GATING INHIB switches: 04.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 1.666±0.010.
8		REPLIES GATING PASS switches: 07. REPLIES GATING INHIB switches: 03.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 1.428±0.010.
9		REPLIES GATING PASS switches: 08. REPLIES GATING INHIB switches: 02.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 1.250±0.010.
10		REPLIES GATING PASS switches: 09. REPLIES GATING INHIB switches: 01.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 1.111±0.010.
11	FUNCTION switch PERIOD B x M 10^4.	REPLIES GATING PASS switches: 10. REPLIES GATING INHIB switches: 90.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 10.000±O.O1O.
12		REPLIES GATING PASS switches: 20. REPLIES GATING INHIB switches: 80.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 5.000 ±O.O1O.
13		REPLIES GATING PASS switches: 30. REPLIES GATING INHIB switches: 70.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 3.333 ±O.O1O.
14		REPLIES GATING PASS switches: 40. REPLIES GATING INHIB switches: 60.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 2.500±0.010.
15		REPLIES GATING PASS switches: 50. REPLIES GATING INHIB switches: 50.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 2.000±0.010.
16		REPLIES GATING PASS switches: 60. REPLIES GATING INHIB switches: 40.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 1.666±0.010.
17		REPLIES GATING PASS switches: 70. REPLIES GATING INHIB switches: 30.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 1.428±0.010.

Table 3–27. Variable Gating Functional Testt-Continued

step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
18		REPLIES GATING PASS switches: 80. REPLIES GATING INHIB switches: 20.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication,	Frequency counter indication is 1.250±0.010.
19		REPLIES GATING PASS switches: 90. REPLIES GATING INHIB switches: 10.	Momentarily press frequency counter RESET switch and after two gating periods, observe frequency counter indication.	Frequency counter indication is 1.111±0.010.

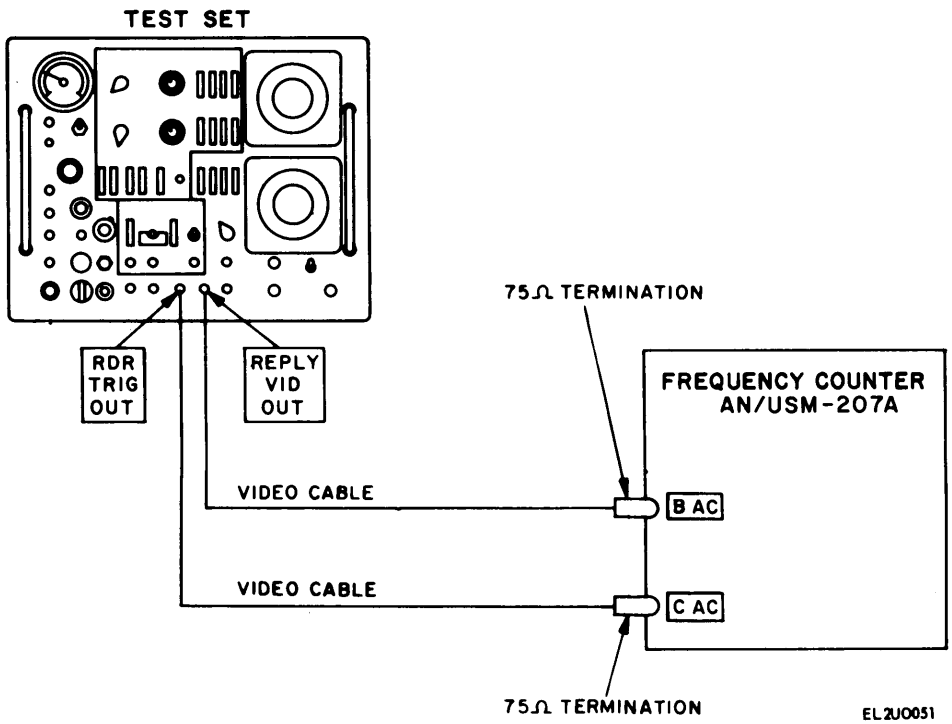

Figure 3-33. Variable gating test setup.

Table 3–28, Mode 4 Challenge Video and GTC Trigger Functioal Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–34 Set up oscilloscope paragraph 3–4c, except set controls as follows:	Set up test set paragraph *3–4b.*	Adjust oscilloscope DIV DELAY control to observe mode 4 challenge video pulse train.	Total number of pulses is 36 (4 sync pulses, one blank pulse position and 32 information pulses).

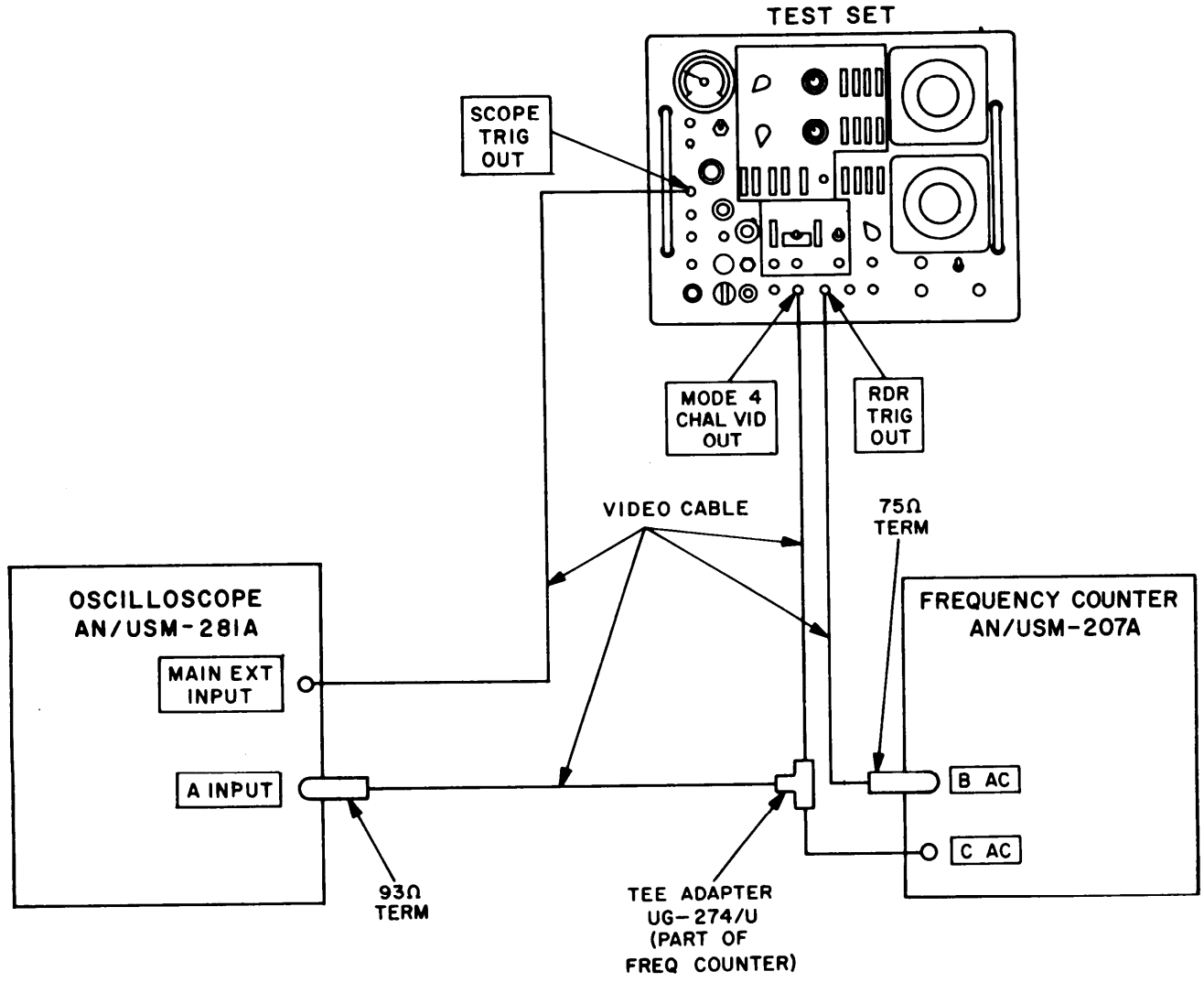

Figure 3-34 Mode 4 challenge video test setup.

Table 3–28. Mode 4 Challenge Video and GTC Trigger Functional Test-Continued

Step No.	Control settings: Test equipment	Control settings: Test set	Test procedure	Performance standard
1 (cont.)	MAIN TIME/DIV switch: 50 µSEC. DELAYED TIME/DIV switch: IOµSEC. Sweep display switch: DELAYED.			

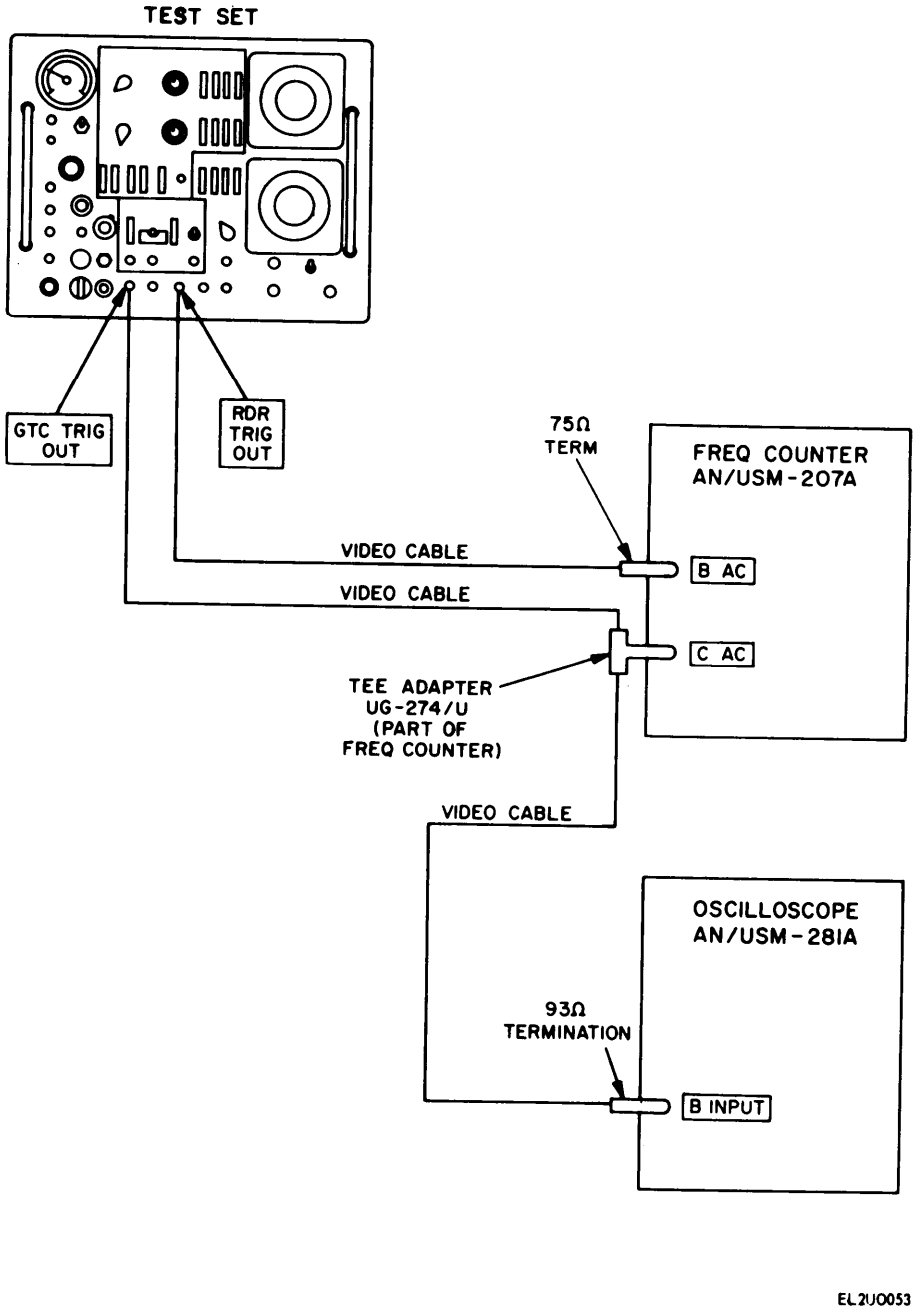

Figure 3–35. Mode 4 GTC trigger test setup,

step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (cont.)	Set up frequency counter, paragraph 3–4e and as follows: FUNCTION switch: TIME B→ C. Time base switch: 1 0'. B and C SLOPE switches: +. B and C TRIGGER controls: +2. B MULTIPLIER switch: 3. C MULTIPLIER switch: 1. COM/SEP switch: SEP.			
2	Set oscilloscope DELAYED TIME/DIV switch:.1 µSEC.		Adjust oscilloscope DIV DELAY control to observe one pulse. *a.* Measure pulse amplitude. *b.* Measure pulse width at 50'% of pulse amplitude.	a. Pulse amplitude is 5.0 ±0.5 volts. *b.* Pulse width is 0.5 ±0.05 µsec.
3			Observe frequency counter indication.	Frequency counter indicates 182.5 ±0.6 µsec.
4	Connect test setup as shown in figure 3–35.		Observe frequency counter indication.	Frequency counter indicates 386.5 ±0.6 µsec.
5			Adjust oscilloscope DIV DELAY control to observe GTC TRIG. a. Using oscilloscope, measure pulse amplitude. *b.* Measure pulse width at 50% of pulse amplitude.	a. 5.0 ±0.5 volts. *b.* Pulse width is 0.8 ±0.2 µsec.

Table 3–29. *Rf Output Frequency Functional Test*

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–36, Set up oscilloscope, paragraph 3–4c. Set up frequency comparator, paragraph *3–4f* Set up frequency counter, paragraph 3–4e except set the controls as follows:	Set up test set, paragraph *3-4b*, except set controls as follows: REPLIES MODULATION SEL switch: CW. SUM ATTEN control: -l0	*a.* Adjust frequency comparator FREQUENCY MEGACYCLES COARSE VERNIER AND FINE VERNIER from 216 to 220 MHz until a zero beat is indicated on oscilloscope A INPUT. *b.* Observe frequency counter indication. Using the following formula determine the test set center frequency. f = (200 MHz + counter reading in MHz X 5)	*a.* None, *b.* Frequency is 1090 MHz ±0.01%.

Table 3-29. Rf Output Frequency Functional Test-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (cont.)	SENSITIVITY switch: PLUG-IN. FUNCTION switch: FREQ. DISPLAY control: as required. POWER switch: STORE. FREQUENCY TUNING–MC switch: 200. INPUT switches: 10V MAX/10V MAX. DIRECT/HETRO-DYNE switch: HETRODYNE. Time base switch: 1.		**NOTE** Use oscilloscope delay sweep as necessary to align zero beat with marker pulse.	
2	Oscilloscope: DIS-PLAY switch: ALT. B INPUT VOLTS/ DIV switch: 2. DELAY TIME/DIV switch: 1 @EC.	SIG GEN FUNCTION switch: SWP ± 5 MHZ.	*a.* Observe markers on B INPUT are are shown in figure 2–8.	a. Five markers appear on B INPUT.
			b. Adjust frequency comparator FREQUENCY MEGACYCLES control from 216 to 218 MHz until zero beat on A INPUT is aligned with leading edge of 1st (1085 MHz) marker on B INPUT.	*b.* None.
			c. Observe frequency indication on frequency counter.	*c.* None.
			d. Using formula in step 1, deter-mine frequency of marker.	*d.* Frequency is 1084.9 to 1085.1 MHz.
3			*a.* Adjust frequency comparator FREQUENCY MEGACYCLES controls from 217 to 219 MHz until zero beat on A INPUT is aligned with leading edge of 2nd marker.	*a.* None.
			b, Observe frequency comparator indication.	*b.* None.
			c. Using formula in step 1, deter-mine frequency of marker.	*c.* Frequency is 1088.9 to 1089.1 MHz.
4			*a.* Adjust frequency comparator FREQUENCY MEGACYCLES controls from 217 to 219 MHz until zero beat is aligned with leading edge of 3rd marker.	*a.* None.
			b. Observe frequency counter indi-cation. Using formula in step 1, determine frequency of marker.	*b.* Frequency is 1089.9 to 1090.1 MHz.

Table 3–29. Rf Output Frequency Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
5			*a.* Adjust frequency comparator FREQUENCY MEGACYCLES controls from 217 to 219 MHz until zero beat is aligned with leading edge of 4th marker.	*a.* None.
			b. Observe frequency marker indication. Using formula in step 1, determine frequency of marker.	*b.* Frequency is 1090.9 to 1091.1 MHz.
6			*a.* Adjust frequency comparator FREQUENCY MEGACYCLES controls from 218 to 221 MHz until zero beat is aligned with leading edge of 5th marker.	*a.* None.
			b. Observe frequency counter indication. Using formula in step 1, determine frequency of marker.	*b.* Frequency is 1094.9 to 1095.1 MHz.
7	Oscilloscope: MAIN TIME/DIV switch: 2 MSEC.	SIG GEN FUNCTION switch: SWP ±15 MHZ.	Observe markers on B INPUT areas shown in figure 2–9.	Display contains nine markers.
8			*a.* Adjust frequency comparator FREQUENCY MEGACYCLES controls from 214 to 216 MHz until zero beat is aligned with leading edge of 1st marker.	*a.* None,
			b. Observe frequency counter indication. Using formula in step 1, determine frequency of marker.	*b.* Frequency is 1074.7 to 1075.3 MHz.
9			*a.* Adjust frequency . comparator FREQUENCY MEGACYCLES controls from 215 to 217 MHz until zero beat is aligned with leading edge of 2nd marker.	*a.* None.
			b. Observe frequency counter indication. Using formula in step 1, determine frequency of marker.	*b.* Frequency is 1079.7 to 1080.3 MHz.
			NOTE 3rd through 7th markers were checked previously.	
10			*a.* Adjust frequency comparator FREQUENCY MEGACYCLES controls from 219 to 221 MHz until zero beat is aligned with leading edge of 8th marker.	*a.* None.
			b. Observe frequency counter indication. Using formula in step 1, determine frequency of marker.	*b.* Frequency is 1099.7 to 1100.3 MHz.
11			*a.* Adjust frequency comparator FREQUENCY MEGACYCLES controls from 220 to 222 MHz until zero beat is aligned with leading edge of 9th marker.	*a.* None.

Table 3–29. Rf Output Frequency Functional Test-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
11 (cont.)			*b.* Observe frequency counter indication. Using formula in step 1, determine frequency of marker.	*b.* Frequency is 1104.7 to 1105.3 MHz.
12	A VOLTSDIV switch: 005.	REPLIES MODULATION SEL switch: 30 KHZ.	*a.* Connect Square Law Detector RF–210/U from test set SUM RF IN/OUT jack to oscilloscope A INPUT.	*a.* None.
			b. Locate 30 kHz pulse with most amplitude between first and ninth marker pulses.	*b,* None.
			c. Using oscilloscope A POSITION control, reference peak of 30 kHz pulse on line of oscilloscope graticule.	*c.* None.
			d. Locate 30 kHz pulse with least amplitude between first and ninth marker pulses.	d. None.
			e. Adjust SUM ATTEN control until pulse peak is at reference of step 12c above.	*e.* SUM ATTEN control setting is between -9 and -lOd B.

Table 3–30. Rf Output Power Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3–37. Set up rf power meter, paragraph *3–4i.* Set up pulse power calibrator set, paragraph 3–4k.	Set up test set, paragraph *3-4b,* except set controls as follows: REPLIES MODULATION SEL switch: CW. SUM ATTEN control: *-20.* DIFF INTERLEAVE/ ATTEN control: -20.	In accordance with the rf power measurement procedure outlined in TM 11–66225– 1549– 12 determine cw rf output power.	Rf output power is -20 ±1.0 dBm.
2		SUM ATTEN control: -10.	Determine rf output power.	Rf output power is *-10 ±1.0* dBm.
3		SUM ATTEN control: 0.	Determine and note rf output power.	Rf output power is *0* ±1.0 dBm.
4		REPLIES MODULATION SEL switch: M4–3P.	*a.* Disconnect bolometer from test set SUM RF IN/OUT jack and connect pulse power calibrator set R.F. INPUT jack to test set SUM RF IN/OUT jack.	a. None.
			b. Using specific operating instructions in TM 11–6625–402–15 only, determine rf power at pulse power calibrator set R.F. INPUT jack.	*b.* None.

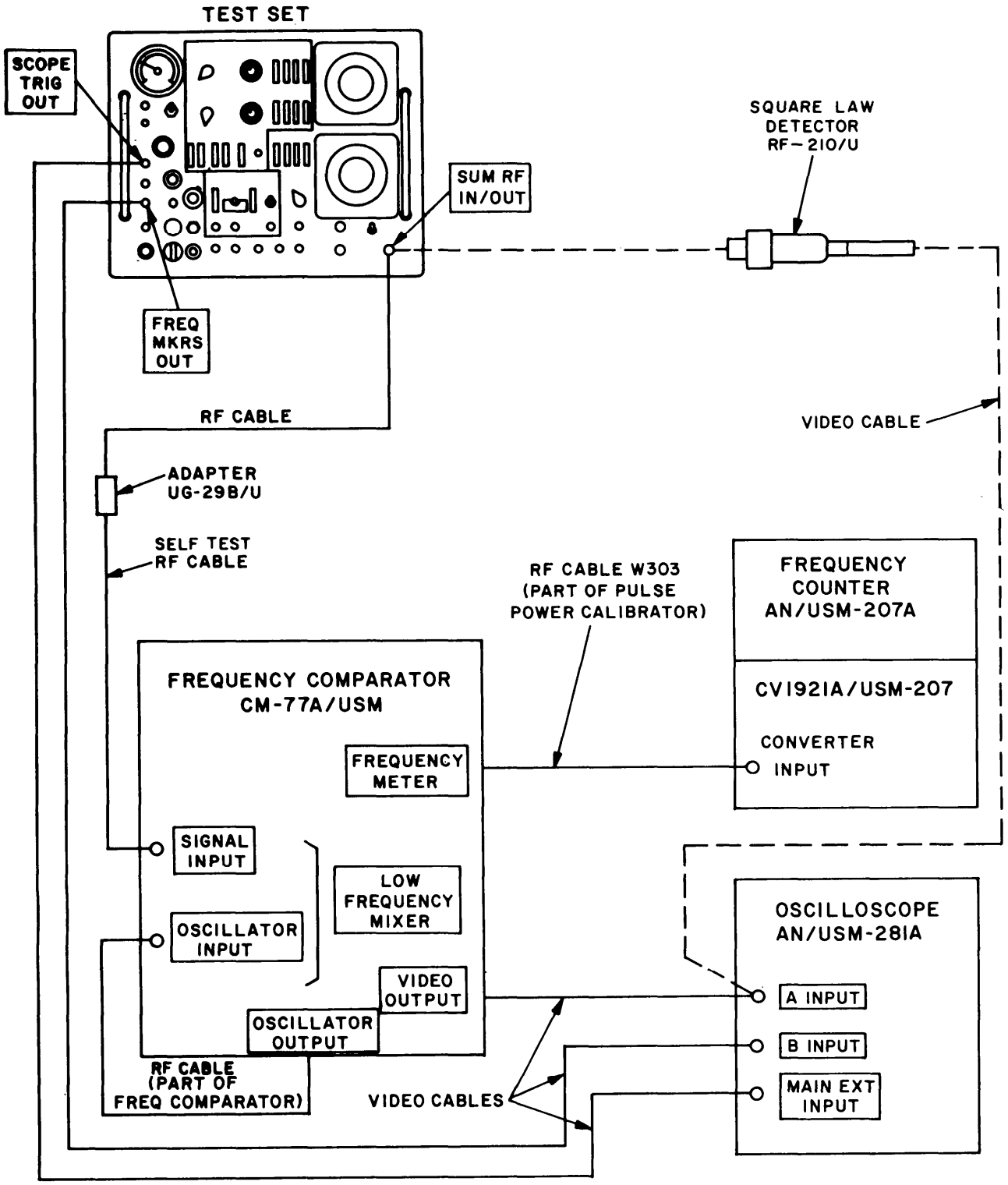

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figure 3-36. RF output frequency test setup.

Table 3–30. Rf Output Power Functional Test—Continued

step No.	Control settings: Test equipment	Control settings: Test set	Test procedure	Performance standard
4 (Cont.)			*c.* Subtract cable loss of cable connected to pulse power calibrator R.F. INPUT jack from indication of step *b.*	*c.* Power output is 0 ±1.0dBm,
5			*a.* Determine difference between power levels noted in steps 3 and 4c. This is cw to peak pulse power difference at test set SUM RF IN/OUT jack.	*a.* Power difference is 1.0 dB max.
			b. Disconnect cable from test set SUM RF IN/OUT jack,	*b.* None.
6	Pulse power calibrator set TRIGGER NO. 1 switch: OFF.	REPLIES MODULATION SEL switch: CW. DIFF/INTERLEAVE ATTEN control: -20.	Connect input of bolometer to test set DIFF RF IN/OUT jack. Determine rf output power.	RF output power is -20 ±1.0 dBm.
7		DIFF/INTERLEAVE ATTEN control: -10.	Determine rf output power,	RF output power is -10 ±1.0 dBm.
8		DIFF/INTERLEAVE ATTEN control: -O.	Determine and note rf output power.	RF output power is 0 ±1.0 dBm.
9		REPLIES MODULATION SEL switch: M4–3P.	*a.* Disconnect bolometer from test set DIFF RF IN/OUT jack. Connect pulse power calibrator set R.F. INPUT jack to DIFF RF IN/OUT jack.	**a.** None.
			b. Repeat steps *4b* and *4C* and note power output.	**b.** Power output is 0 ±1.0 dBm.
10			Determine difference between power levels in steps 8 and 9. This is the cw to peak power difference of test set DIFF RF IN/OUT jack.	Power difference is 1.0 dB max.

Table 3–31. Modulutor and Demodulator Functional Test

Step No.	Control settings: Test equipment	Control settings: Test set	Test procedure	Performance standard
1	Connect test setup as shown in figure 3–38. Set up oscilloscope, paragraph 3–4c and as follows: A polarity switch: -UP. A VOLTS/DIV switch: .005. A AC/GND/DC switch: AC.	Set up test set, paragraph *3–4b* except: SUM ATTEN control: -10. DIFF/INTERLEAVE ATTEN control: -10.	Observe that eight pulses are present. Adjust oscilloscope DIV DELAY control to position intensified trace over 2nd pulse.	Eight pulses are present.

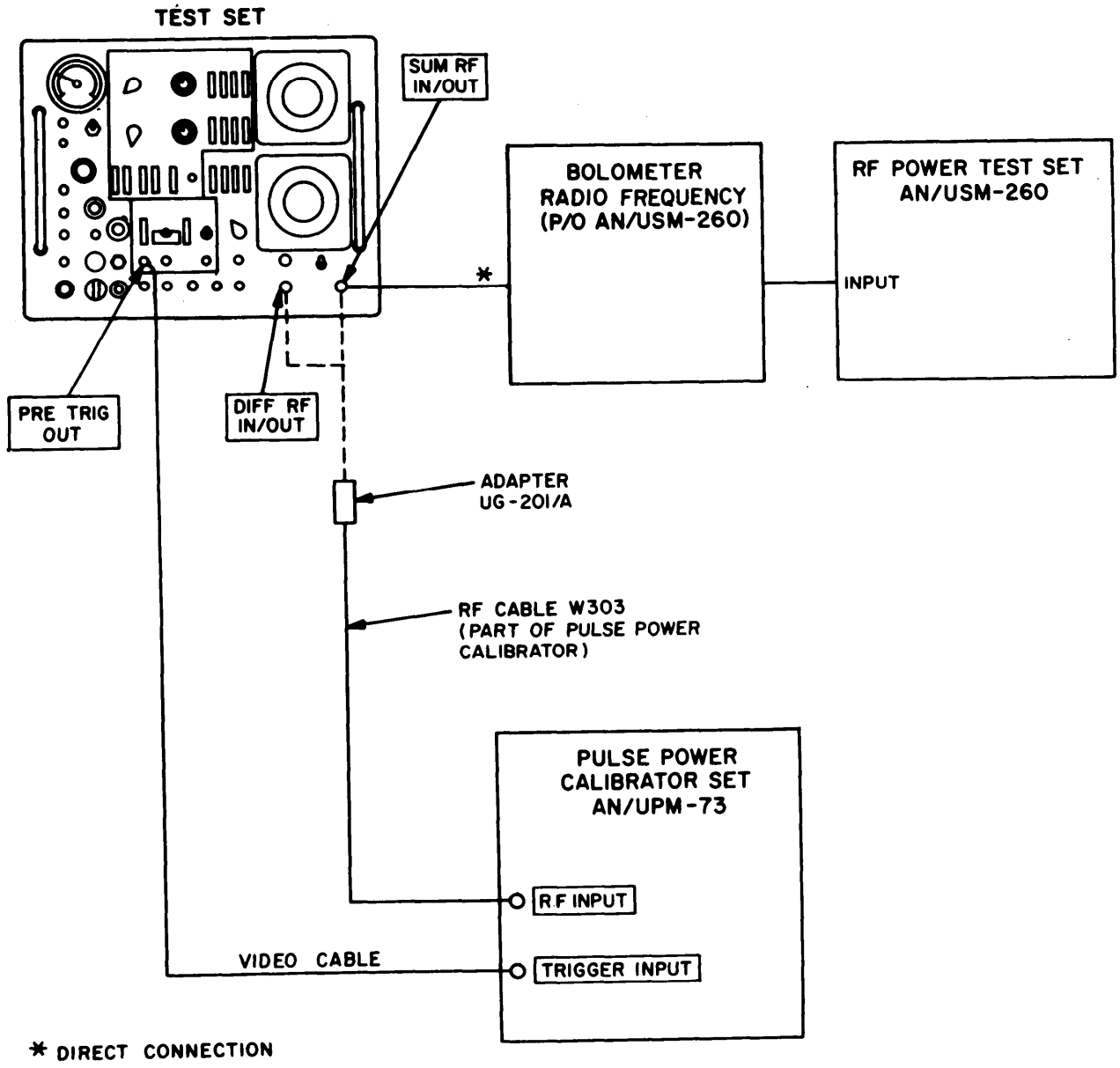

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Figure 3-37. Rf output power test setup.

Table 3-31. Modukator and Demodulator Functional Test-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (cont.)	DISPLAY switch: ALT. MAIN TIME/DIV switch: 50 µSEC. DELAYED TIME/DIV switch: .1 µSEC.			

Table 3–31. Modulator and Demodulator Functional Test-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
2	Oscilloscope: SWEEP display switch: DE-LAYED.		Using 0.1 µsec markers measure and record pulse width at 50% amplitude points. Record pulse width.	Pulse width is 0.45 ± 0.05 µsec.
3			Measure pulse rise time at the 1% and 81% amplitude points, Record results.	Pulse rise time is 0.05 to 0.1 µsec.
4			Measure and record pulse fall time. Record results.	Pulse fall time is 0.05 to 0.2 µsec.
5	Oscilloscope: A VOLTS/DIV switch: .2. A POLARITY switch: +UP.	MEASUREMENT FUNCTION SEL switch: PWR.	*a.* Disconnect square law detector from test set SUM RF IN/OUT jack and oscilloscope A INPUT jack. Connect self-test rf cable between test set SUM RF IN/OUT jack and LOW PWR IN jack and connect test set DEMOD VID OUT jack to oscilloscope A INPUT jack (with 75 ohm termination).	*u* None.
			b. Adjust test set DEMOD VID LEVEL control for 1.0 volt pulse amplitude.	*b.* None.
			c. Measure pulse width.	*c.* Pulse width is within ±0.02 µsec of width recorded in step 2.
6	**Oscilloscope:** A VOLTS/DIV switch. 1		Adjust oscilloscope A INPUT VOLTS/DIV vernier control for a pulse amplitude of 8 divisions. Using the oscilloscope CRT graticule, measure distance in divisions between 1% and 81% amplitude points, on rising and falling edges.	Pulse rise and fall times are within 0.02 µsec of times recorded in steps 3 and 4.
7	Oscilloscope: A VOLTS/DIV switch: .005. A VOLTS/DIV vernier control: CAL: A POLARITY switch: -UP.		a. Disconnect cable and termination from oscilloscope A INPUT jack.	*a.* None.
			b. Connect square law detector between test set DIFF RF IN/OUT jack and oscilloscope A INPUT jack and repeat steps 1 through 4.	*b.* Same as steps 1 through 4.

Table 3–32. Rf Input Power Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure *3–39*. Set up pulse power calibrator, paragraph *3–4k*.	Set up test set paragraph *3–4b* except as follows: MEASUREMENT FUNCTION SEL switch: PWR.	Perform SPECIFIC OPERATING INSTRUCTIONS (external trigger) steps (1) through (29), section 4, paragraph 3, TM 11 –6625–402-15.	20 dBw (50 dBm) minimum. **NOTE** This is the output of the interrogator set less the attenuation of rf cable.

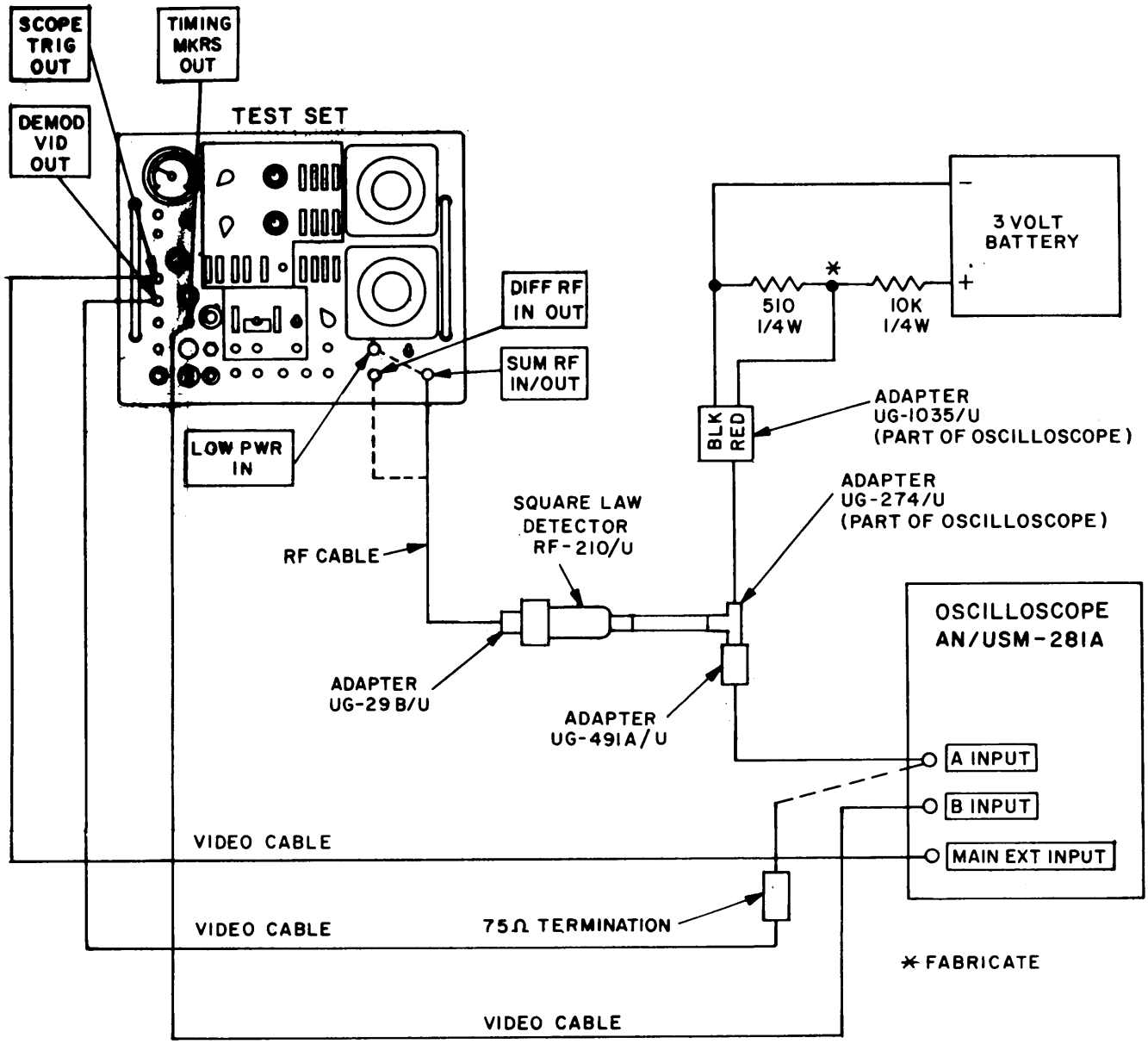

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Figure 3–38 Modulator and demoduluator test setup.

Table 3–32. Rf Input Power Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (Cont.)	Set up oscilloscope, paragraph 3–4c and as follows: A INPUT VOLTS/ DIV switch: .2.	PRT SEL (μSEC switch: 2500. DIFF/INTERLEAVE control: -20 dB.	CAUTION To prevent damage to equipment, release control box CHALLENGE switch instead of performing step (30). Then per-	

Table 3–32. Rf Input Power Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (Cont.)	MAIN TIME/DIV switch: .1 MSEC. DELAYED TIME/ DIV switch: 1 µSEC. Set up interrogator set and power supply, paragraph 3–4 *l*, and as follows: CHALLENGE switch held to ON.		form steps (31) through (37) then hold CHALLENGE switch to ON to perform steps (38) through (40). This determines rf pulse power at pulse power calibrator R.F. INPUT jack. Convert final CALIBRATED ATTENUATOR control indication from dbm to dbw by subtracting 30 dB. Record power level in dBw.	
2	Control box CHALLENGE switch released.		Disconnect rf cable from pulse power calibrator R.F. INPUT jack and connect to test set SUM RF IN/ OUT jack.	
3	Control box CHALLENGE switch held to ON.		a. Adjust test set MEASUREMENT DEMOD VID LEVEL control until 1st pulse displayed on oscilloscope is 1.0 volt in amplitude. *b.* ***Note*** MEASUREMENT meter indication (in dBw). c. By subtraction determine the difference between the MEASUREMENT meter indication *(b* above) and the power level recorded in step 1.	*a.* None. *b.* None. c. The difference is 1.0 dB maximum.
4	control box CHALLENGE switch released,		Exchange cables between test set SUM RF IN/OUT and DIFF RF IN/OUT jack.	
5	Control box CHALLENGE switch held to ON.		Repeat step 3.	The difference is 1.0 dB maximum.
6	Control box: POWER switch: OFF. Power supply: AC and DC power switches: OFF.		Disconnect test set up.	
7	Set up pulse generator, paragraph *3–4h* and for a +20 volt pulse with a duration of 7 µsec. Set up signal generator, paragraph *3–4j* and as follows: FREQUENCY control: 1030 MHz. ATTENUATOR control: 0.00 DB		*a.* Connect test set up shown in figure3–11. *b,* Set up rf signal generator to apply -12 dBm to test set LOW PWR IN jack as described in paragraph 3– 109(2) (e), *(f* and (g).	

Table 3-32. Rf Input Power Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
7 (Cont.)	ON/OFF switch pressed. RF switch: pressed. ALC switch: released. SQ WAVE switch released. PULSE switch: pressed. AM switch: released. FM switch: released. Pulse power calibrator: TRIGGER NO. 1 switch: ON. TRIGGER switch: INT.			
8	Pulse power calibrator: TRIGGER NO. 1 switch: OFF.		*a.* Disconnect rf cable from pulse power calibrator R.F. INPUT and connect to test set LOW PWR IN jack.	a. None.
			b. Set pulse power calibrator TRIGGER NO. 1 switch to ON.	*b.* None.
			c. Adjust test set DEMOD VID LEVEL control until pulse (displayed on oscilloscope) is 1.0 volt in amplitude.	c. None.
			d. Observe test set MEASUREMENT meter power indication.	*d.* Meter indicates +18 ±1 dBw.
9	Pulse power calibrator: TRIGGER NO. 1 switch: OFF. CALIBRATED ATTENUATOR control: 030+DB (+3 dBm).		*a.* Disconnect rf cable from 15 dB attenuator and connect to pulse power calibrator R.F. INPUT jack.	
			b. Set pulse power calibrator TRIGGER NO. 1 switch to ON.	
			c. Adjust rf signal generator ATTENUATION (DB) control until output pulse observed on pulse power calibrator is at level of reference line.	
			d. Remove attenuator from test set LOW PWR IN jack.	
10	Pulse power calibrator: TRIGGER NO. 1 switch: OFF.		*a.* Disconnect rf cable from pulse power calibrator RF INPUT jack and connect to test set LOW PWR IN jack.	*a.* None.
			b. Set pulse power calibrator TRIGGER NO. 1 switch to ON.	*b.* None.
			c. Adjust test set DEMOD VID LEVEL control until pulse (on oscilloscope) amplitude is 1.0 volt.	*c.* None.

Table 3–32. Rf Input Power Functinal Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
10 (cont.)			*d.* Observe test set MEASUREMENT meter indication.	*d*. Meter indicates +33 ±1 dBw.
11	Pulse power calibrator TRIGGEE NO. 1 switch: OFF. CALIBRATED ATTENUATOR control: 000 -DE (OdBm).		*a*. Disconnect rf cable from test set LOW PWR IN jack and connect to pulse power calibrator R.F. INPUT jack. *b*. Set pulse power calibrator TRIGGER NO. 1 switch to ON c. Adjust rf signal generator ATTENUATION (DB) control until output pulse on pulse power calibrator is at level of reference line.	
12	Pulse power calibrator: TRIGGER NO. 1 switch: OFF.		*a*. Disconnect rf cable from pulse power calibrator R.F, INPUT jack and connect to test set LOW PWR IN jack. *b*. Set pulse power calibrator TRIGGER NO. 1 switch to ON. *c*. Adjust test set DEMOD VID LEVEL control until pulse (on oscilloscope) amplitude is 1.0 volt. *d*. Observe test set MEASUREMENT meter indication.	a. None. *b*. None. c. None. *d*. Meter indicates +30 ±1 dBw.

Table 3–33. Rf Input Frequency Measurement Functional Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test set up as shown in figure 3–40. Set up signal generator, paragraph *3-4j* and as follows: FREQUENCY (MC) control: 1015. ATTENUATION (DB) control: 005. RF switch: pressed, ALC switch: pressed. SQ WAVE, PULSE, AM, FM switches: released. Set up oscilloscope, paragraph 3 –4c except:	Set up test set, paragraph *3–4b* and as follows: SIG GEN FUNCTION switch: SWP ±15 MHZ. MEASUREMENT FUNCTION SEL switch: FREQ.	*a*. Set up signal generator alc by adjusting ALC control until DBM meter indicates 0. *b*. Connect rf cable to signal generator RF POWER OUTPUTS CAL jack. c. Observe markers on B INPUT are as shown in figure 2–9.	*a*. None. *b*. None. c. Nine markers appear on B INPUT.

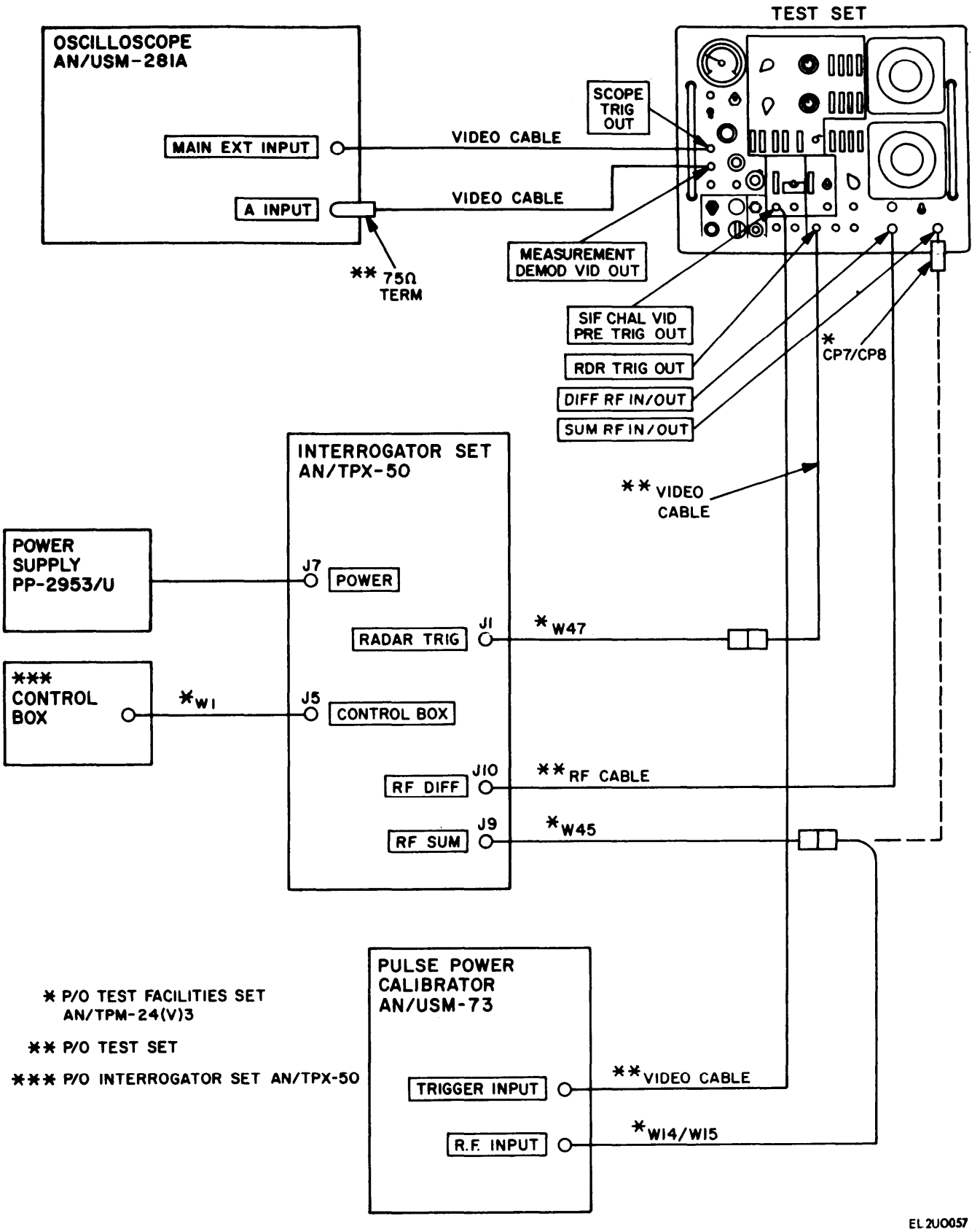

Figure 3-39. Rf input power test setup.

Table 3–33. Rf Input Frequency Measurement Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (Cont.)	DISPLAY switch: DELAYED. MAIN TIME/DIV switch:.2 MSEC. DELAYED TIME/DIV switch: 20 µSEC. Set up frequency comparator, paragraph 3-4f. Set up frequency counter, paragraph 3–4e except: SENSITIVITY switch: PLUG-IN. FUNCTION switch: FREQ. Time base switch: 1. NPUT switches: 10V MAX, DIRECT/HETRODYNE switch: HETRODYNE.			
2	**NOTE** Use oscilloscope delay sweep as necessary to observe signal generator output alignment with marker pulse.		*a.* Adjust signal generator FREQUENCY (MC) control until output on A INPUT is aligned with leading of 1st (1015 MHz) marker on B INPUT.	*a.* None.
			b. Adjust frequency comparator FREQUENCY MEGACYCLES controls from 200 to 205 MHz until zero beat is observed on frequency comparator.	*b.* None.
			c. Observe frequency counter indication. Using following formula calculate marker frequency. f = (200 MHz + counter reading in MHz X 5)	c. Marker frequency is 1015 ± 0.300 MHz.
3			*a.* Adjust signal generator FREQUENCY (MC) control until output on A INPUT is aligned with leading edge of 2nd (1020 MHz) marker on B INPUT.	*a.* None.
			b. Adjust frequency comparator FREQUENCY MEGACYCLES controls from 202 to 207 MHz until zero beat is observed on frequency comparator.	*b.* None.
			c. Observe frequency counter indication. Using formula in step 2c above, calculate marker frequency.	c. Marker frequency is 1020 ± 0.300 MHz.

Table 3–33. Rf Input Frequency Measurement Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
4			*a.* Adjust signal generator FREQUENCY (MC) control until output on A INPUT is aligned with leading edge of 3rd (1025 MHz) marker on B INPUT.	*a.* None.
			b. Ajust frequency comparator FREQUENCY MEGACYCLES controls from 203 to 208 MHz until zero beat is observed on frequency comparator.	b. None.
			c. Observe frequency counter indication. Using formula in step 2c above, calculate marker frequency.	*c.* Marker frequency is 1025 ± 0.100 MHz.
5			*a.* Adjust signal generator FREQUENCY (MC) control until output on A INPUT is aligned with leading edge of 4th (1029 MHz) marker on B INPUT.	*a.* None.
			b. Adjust frequency comparator FREQUENCY MEGACYCLES controls from 205 to 209 MHz until zero beat is observed on frequency comparator.	b. None.
			c. Observe frequency counter indication. Using formula in step 2c above, calculate marker frequency.	*c.* Marker frequency is 1029 ± 0.100 MHz.
6			*a.* Adjust signal generator FREQUENCY (MC) control until output on A INPUT is aligned with leading edge of 5th (1030 MHz) marker on B INPUT.	*a.* None.
			b. Adjust frequency comparator FREQUENCY MEGACYCLES controls from 205 to 208 MHz until zero beat is observed on frequency comparator.	*b.* None.
			c. Observe frequency counter indication. Using formula in step 2c above calculate marker frequency.	. Marker frequency is 1030 ± 0.100 MHz.
7			*a.* Adjust signal generator FREQUENCY (MC) control until output on A INPUT is aligned with leading edge of 6th (1031 MHz) marker on B INPUT.	*a.* None.
			b. Adjust frequency comparator FREQUENCY MEGACYCLES controls from 205 to 208 MHz until zero beat is observed on frequency comparator.	*b.* None.

Table 3-33. Rf Input Frequency Measurement Functional Test—Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Test set		
7 (cont.)			*c.* Observe frequency counter indication. Using formula in step 2c above, calculate marker frequency.	*c.* Marker frequency is 1031 ± 0.100 MHz.
8			*a.* Adjust signal generator FREQUENCY (MC) control until output on A INPUT is aligned with leading edge of 7th (1035 MHz) marker on B INPUT.	*a.* None.
			b. Adjust frequency comparator FREQUENCY MEGACYCLES controls from 205 to 210 MHz until zero beat is observed on frequency comparator.	*b.* None.
			c. Observe frequency counter indication. Using formula in step 2c above calculate marker frequency.	c. Marker frequency is 1035 ± 0.100 MHz.
9			*a.* Adjust signal generator FREQUENCY (MC) control until output on A INPUT is aligned with leading edge of 8th (1040 MHz) marker on B INPUT.	a. None.
			b. Adjust frequency comparator FREQUENCY MEGACYCLES controls from 205 to 210 MHz until zero beat is observed on frequency comparator.	*b.* None.
			c. Observe frequency counter indication. Using formula in step 2c above calculate marker frequency.	*c.* Marker frequency is 1040 ± 0.300 MHz.
10			*a.* Adjust signal generator FREQUENCY (MC) control until output on A INPUT is aligned with leading edge of 9th (1045 MHz) marker on B INPUT.	*a.* None.
			b. Adjust frequency comparator FREQUENCY MEGACYCLES controls from 207 to 212 MHz until zero beat is observed on frequency comparator.	*b.* None.
			c. Observe frequency counter indication. Using formula in step 2c above calculate marker frequency.	*c.* Marker frequency is 1045 ± 0.300 MHz.

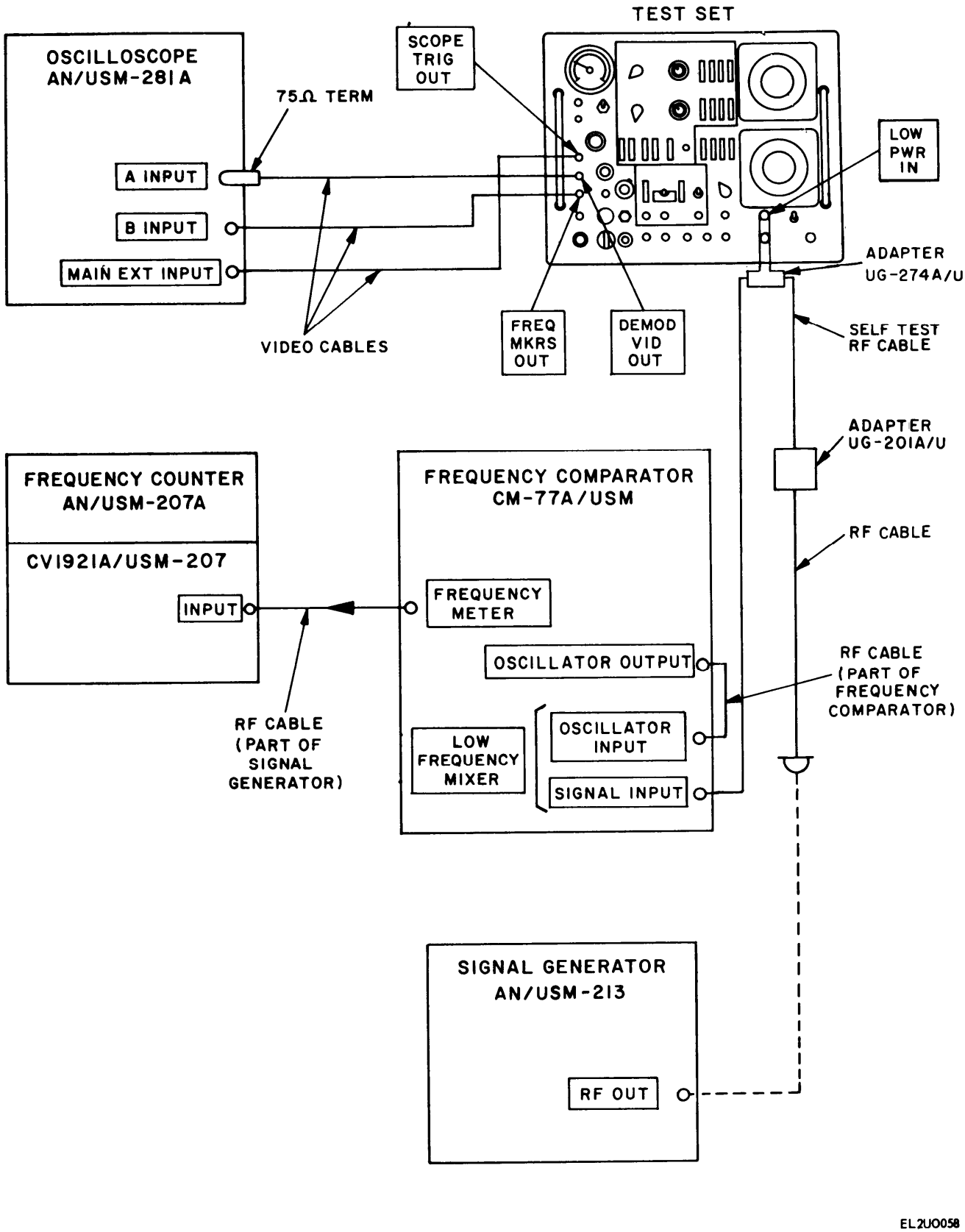

Figure 3-40. Rf input frequency measurement test setup.

APPENDIX

REFERENCES

The following publications contain information applicable to general support maintenance of Radar Test Set AN/TPM–25A.

DAPAM310–4	Index of Technical Manuals, Technical Bulletins, Supply Manuals (Types 7, 8, and 9), Supply Bulletins, and Lubrication Orders.
DAPAM310–7	US Army Equipment Index of Modification Work Orders.
TB SIG 222	Solder and Soldering (TO 31–3–64).
TM 11–5895–687–12	Technical Manual, Operator's and Organizational Maintenance Manual, Interrogator Set AN/TPX–50.
TM 11–6130–233–12	Operator and Organizational Maintenance Manual, Including Repair Parts List, Power Supply PP–2953/U, PP–2953A/U, PP–2953B/U, PP–2953C/U.
TM 11–6625–200–15	Operator, Organizational, DS, GS, and Depot Maintenance Manual, Multimeters ME–26A/U, ME–26B/U, ME–26C/U, and ME–26D/U.
TM 11–6625–368–10	Operator's Manual, Pulse Generator Sets AN/UPM–15 and AN/UPM–15A.
TM 11–6625–402–15	Operator, Organizational, Field, and Depot Maintenance Manual, Pulse Power Calibrator AN/UPM–73.
TM 11-6625–493-15	Operator, Organizational, DS, GS, and Depot Maintenance Manual, Frequency Comparator CM–77A/USM.
TM 11–6625–498–12	Operator and Organizational Maintenance Manual, Test Set, Radio Frequency Power AN/USM–161.
TM 11–6625–537–15	Operator, Organizational, Field, and Depot Maintenance Manual, Voltmeter, Electronic ME–202/U.
TM 11–6625–539–14–3	Operator, Organizational, Direct Support, and General Support Maintenance Manual, Test Set, Transistor TS–1836C/U.
TM 11–6625–700–14–1	Operator, Organizational, Direct Support, and General Support Maintenance Manual, Including Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools), Digital Readout Electronic Counter AN/USM–207A.
TM 11–6625–1517–15	Organizational, DS, GS, and Depot Maintenance Manual, Signal Generator (Hewlett–Packard Model 8614A) AN/USM-213.
TM 11–6625–1703–15	Operator, Organizational, DS, GS, and Depot Maintenance Manual for Oscilloscope AN/USM–281A (Including Repair Parts and Special Tools Lists).
TM 11–6625–2610–12	Technical Manual, Operator and Organizational Maintenance Manual, Radar Test Set AN/TPM–25A.
TM 38–750	The Army Maintenance Management System (TAMMS).

INDEX

* U.S. GOVERNMENT PRINTING OFFICE : 1980 0 - 310-983 (43)

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PUBLICATION NUMBER	DATE	TITLE
TM 11-6625-2610-40	10 AUG 79	Radar Test Set AN/TPM-25A

BE EXACT. . .PIN-POINT WHERE IT IS				IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.	

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PUBLICATION NUMBER	DATE	TITLE
TM 11-5840-340-12	23 Jan 74	Radar Set AN/MPQ-76

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PAGE NO.	PARAGRAPH	FIGURE NO.	TABLE NO.	IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		F03		Zone C 3. On J1-2, change "+24 VDC" to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. + 24 VDC is the input voltage.

TYPED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER
SSG I. M. DeSpiritof 999-1776

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TM 11-6625-2610-40	10 AUG 79	Radar Test Set AN/TPM-25A

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Sig Sec USA Dep (1)
Ft Richardson (CERCOM Oft) (2)
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29-207
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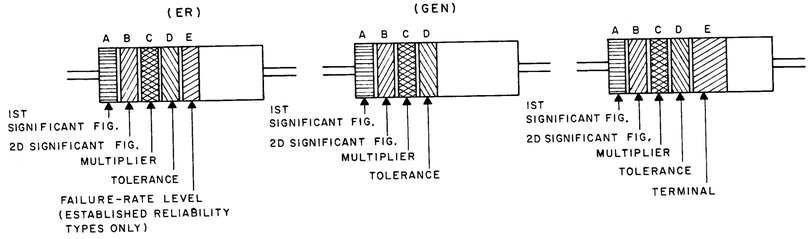
ARNG: None

USAR: None

For explanation of abbreviations used, see AR 310–50.



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS

COLOR-CODE MARKING FOR FILM TYPE RESISTORS

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS) ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL

RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 1ORO = 10.0 OHMS

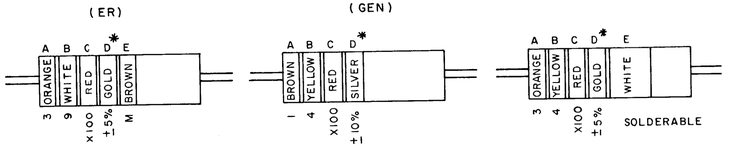
FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED, IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS

TABLE 1
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS

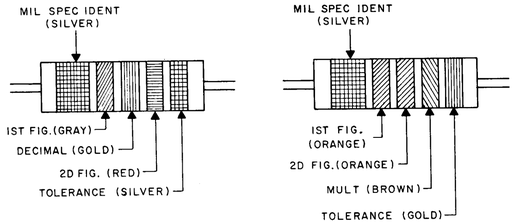
EXAMPLES OF COLOR CODING



COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD



(A) 8.2UH ± 10%

(B) 330UH ± 5%

COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN AT B, THE COLOR BANDS FOR A 330 UH INDUCTOR ARE ILLUSTRATED.

TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN		10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS

EL2U0059

Figure FO-1. Color code for military standard resistors, inductors, and capacitors (sheet 1 of 2).

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM,CN,CY, AND CB.

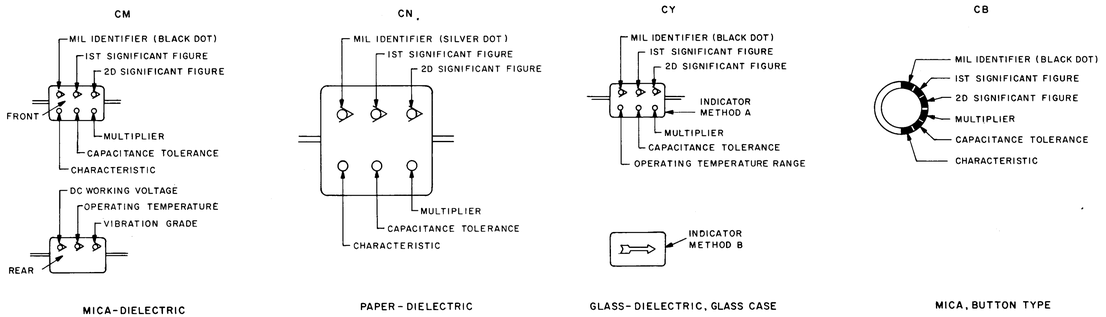
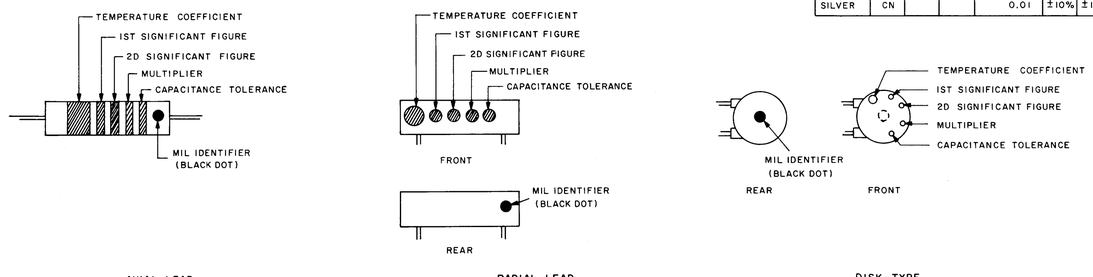


TABLE 3- FOR USE WITH STYLES CM,CN,CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM,CY CB	0	0	1			±20%	±20%		A			-55°TO+70°C	10-55HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55°TO+85°C	
ORANGE		3	3	1,000		30%			D		D	300		
YELLOW		4	4	10,000					E				-55°TO+125°C	10-2,000HZ
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55°TO+150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						

TABLE 4- TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			



1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.
4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE

* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

EL2U0060

Figure FO-1. Color code for military standard resistors, inductors, and capacitors (sheet 2 of 2).

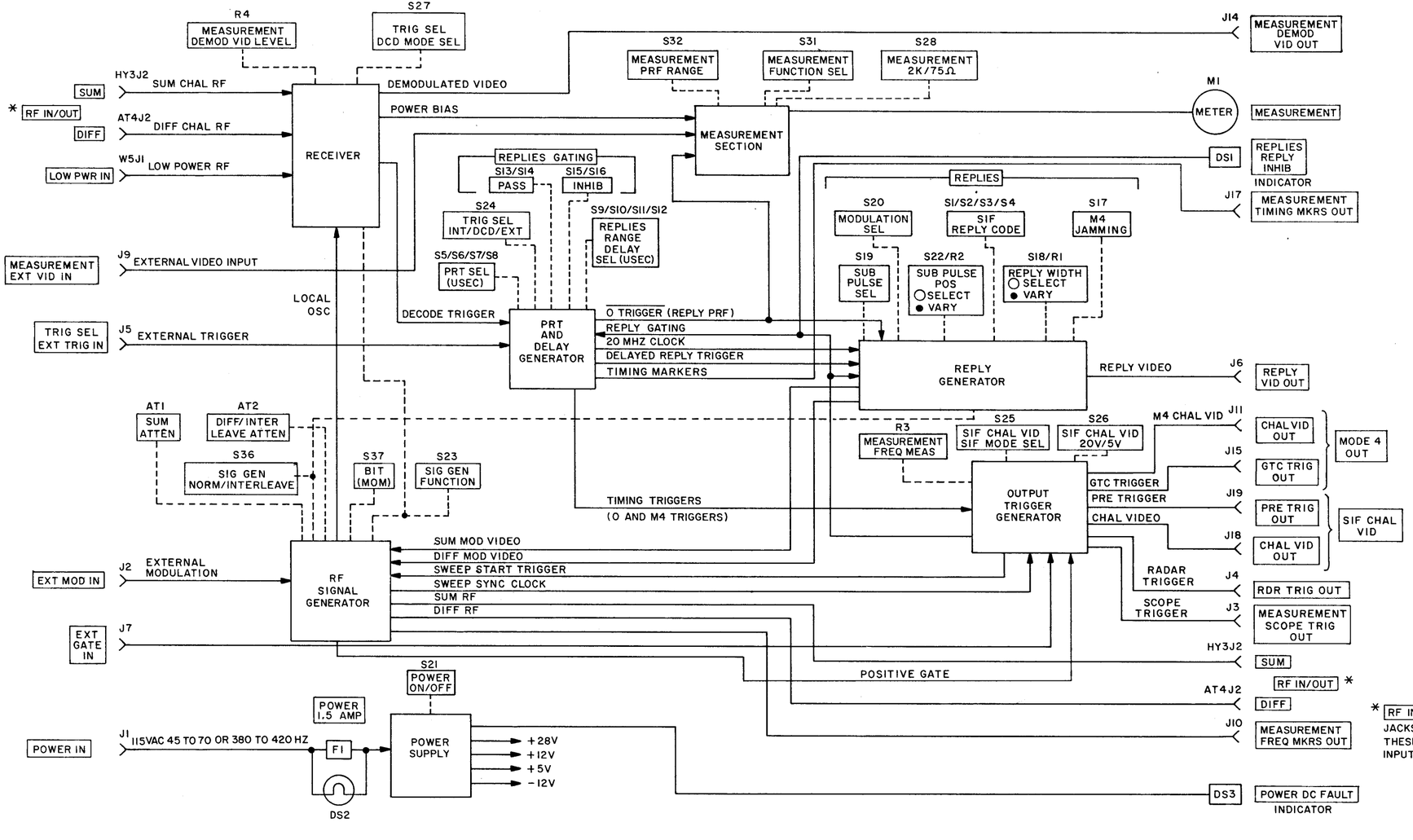
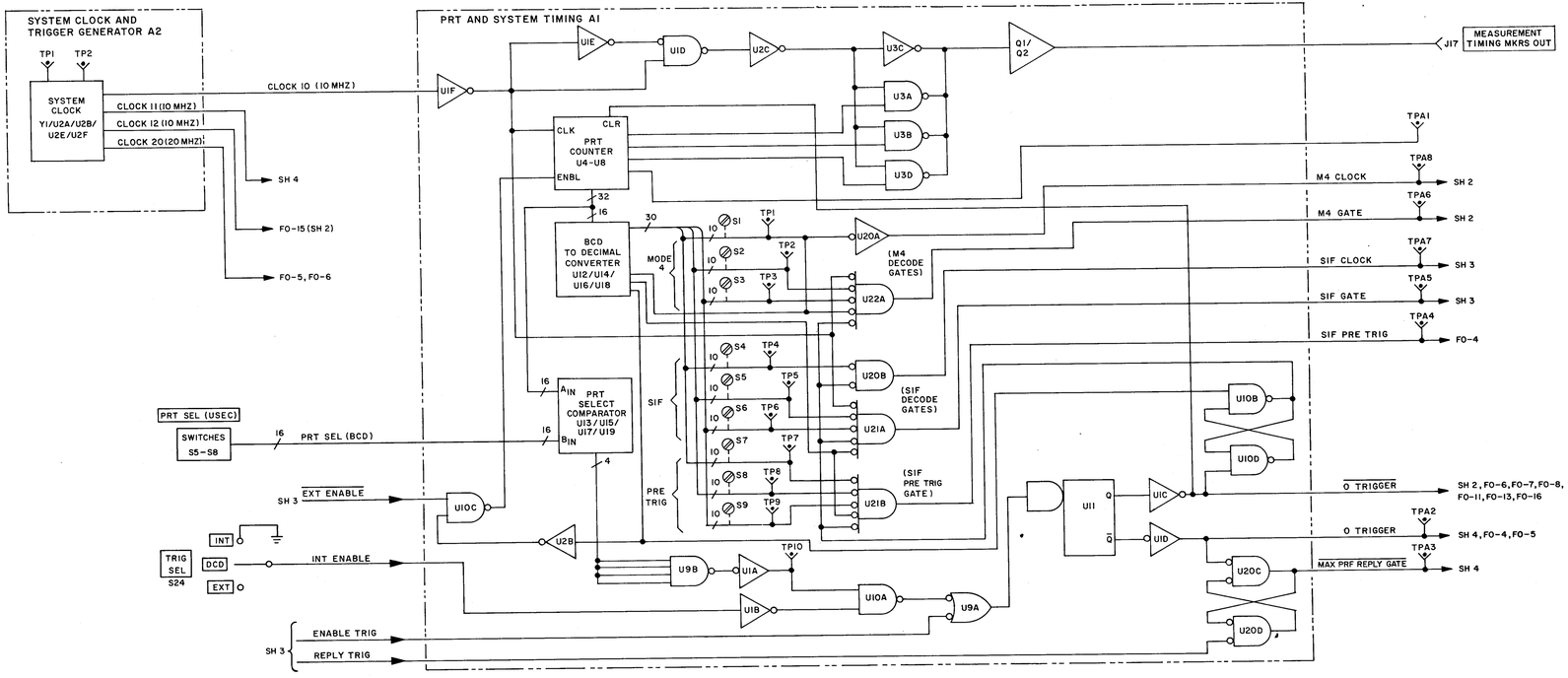
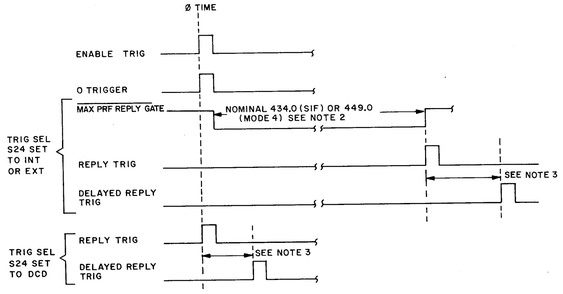


Figure FO-2. Test set, block diagram.



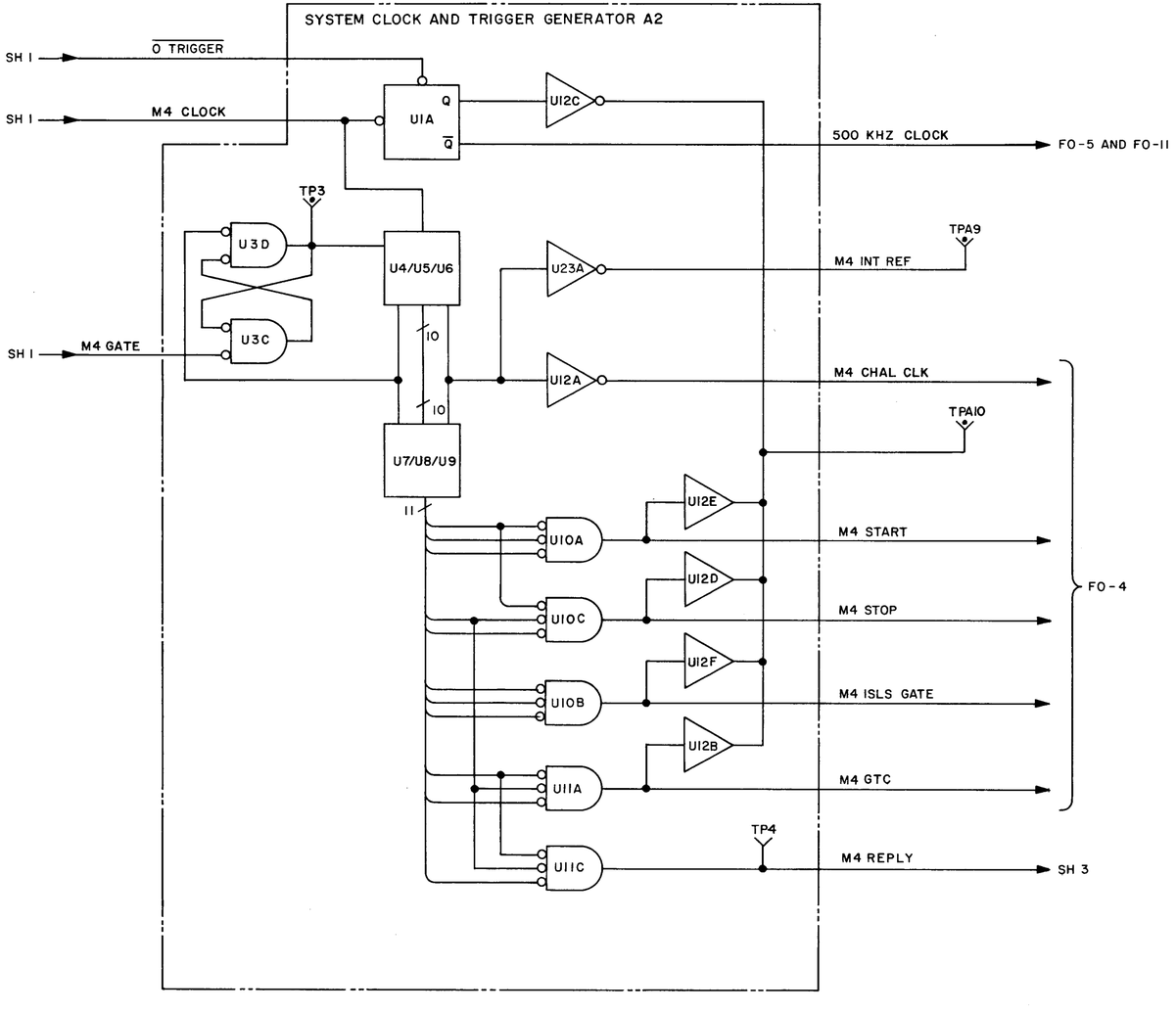


NOTES:

1. ALL TIMES INDICATED IN USEC
2. VARIABLE FROM 360.0 TO 438.0 (SIF) WITH SWITCHES A1S1-S3 AND TERMINALS A1E1-E3 AND 430 TO 459.0 (MODE 4) WITH SWITCHES A1S4-S6; SET FOR DELAY SPECIFIED BETWEEN RDR TRIG OUT AND START OF SIF REPLY OF INTERROGATOR UNDER TEST
3. SPACING DETERMINED BY SETTINGS OF REPLIES RANGE DELAY (USEC) SWITCHES S9-S12

EL2U0062

Figure FO-5. Prt and delay generator, logic diagram (sheet 1 of 4).



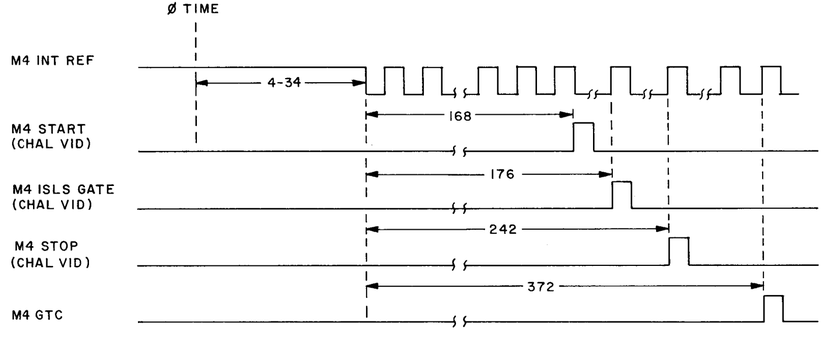


Figure FO-3. Prt and delay generator, logic diagram (sheet 2 of 4).

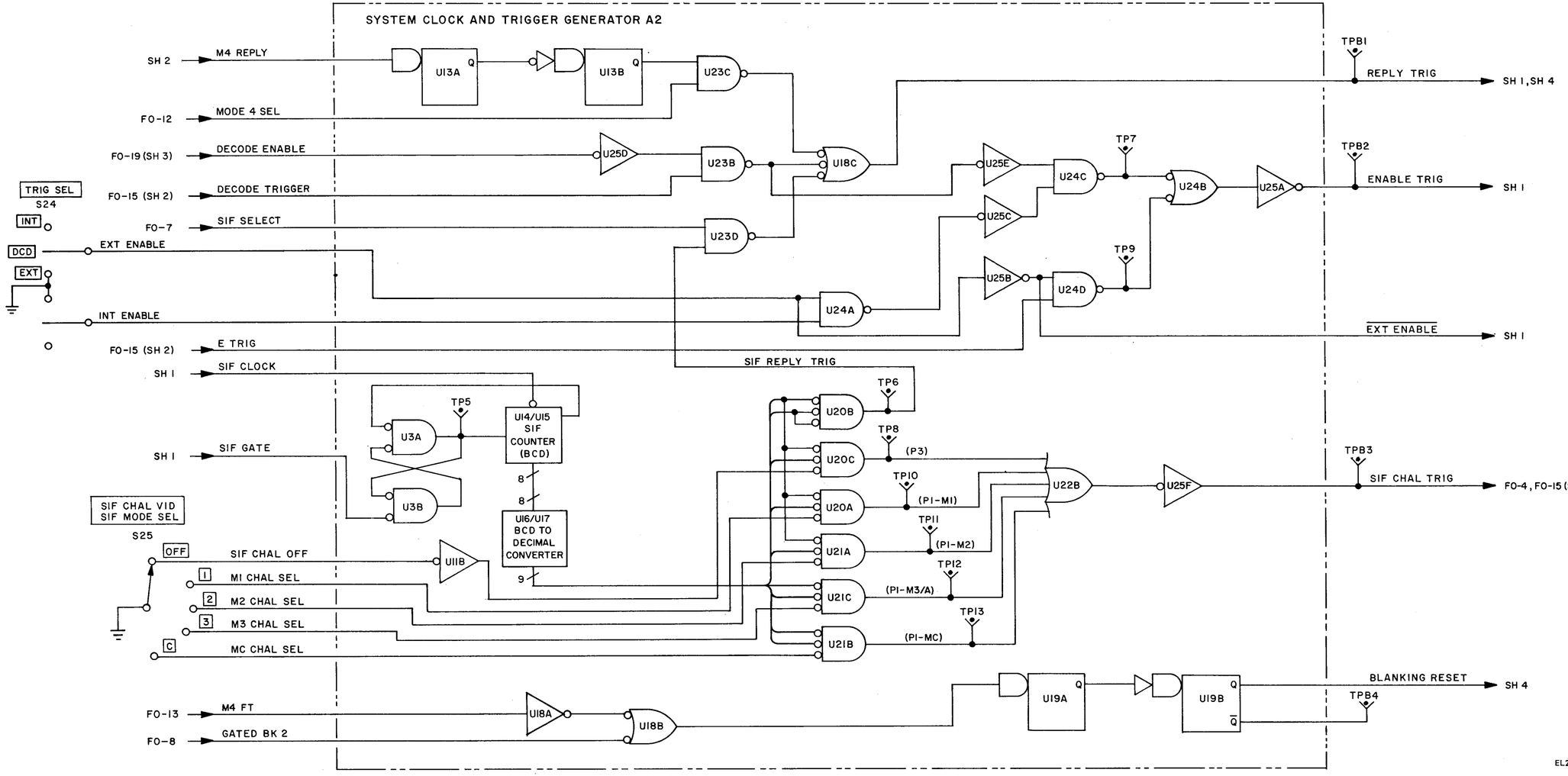


Figure FO-3. Prt and delay generator, logic diagram (sheet 3 of 4).

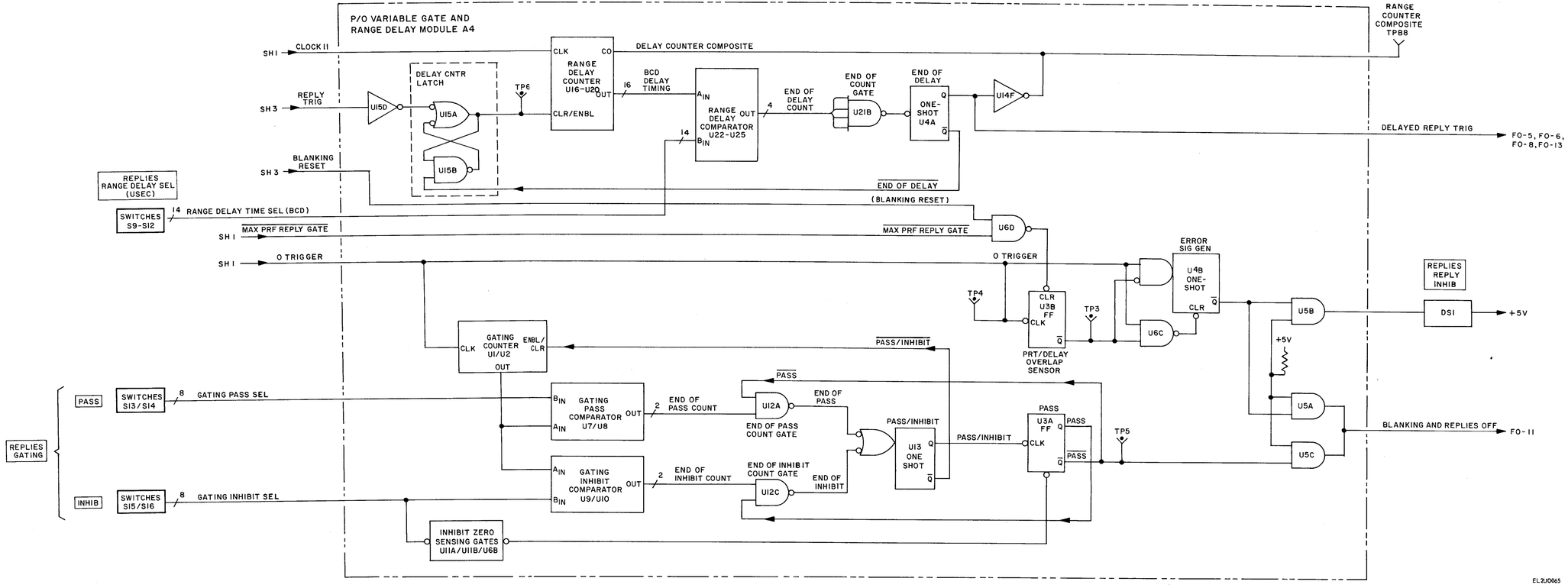


Figure FO-3. Prt and delay generator, logic diagram (sheet 4 of 4).

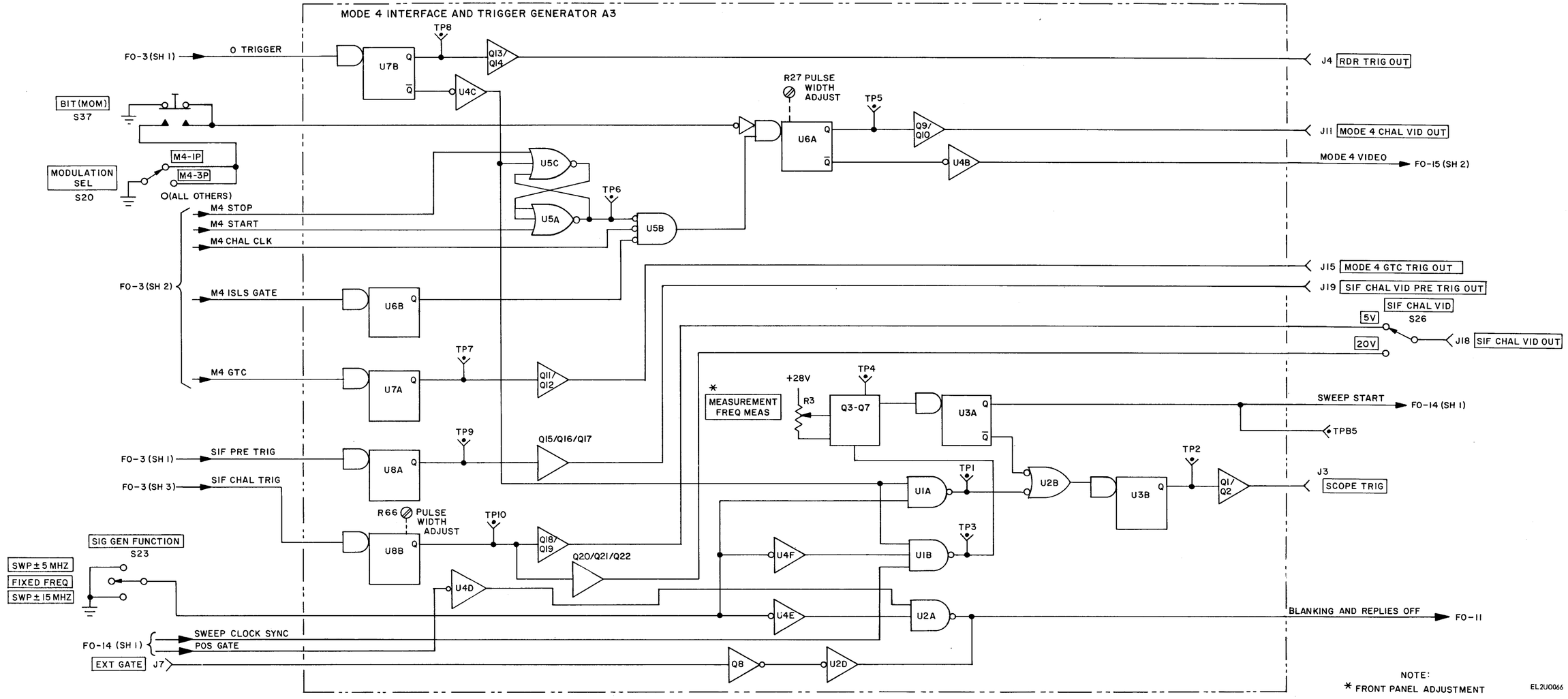
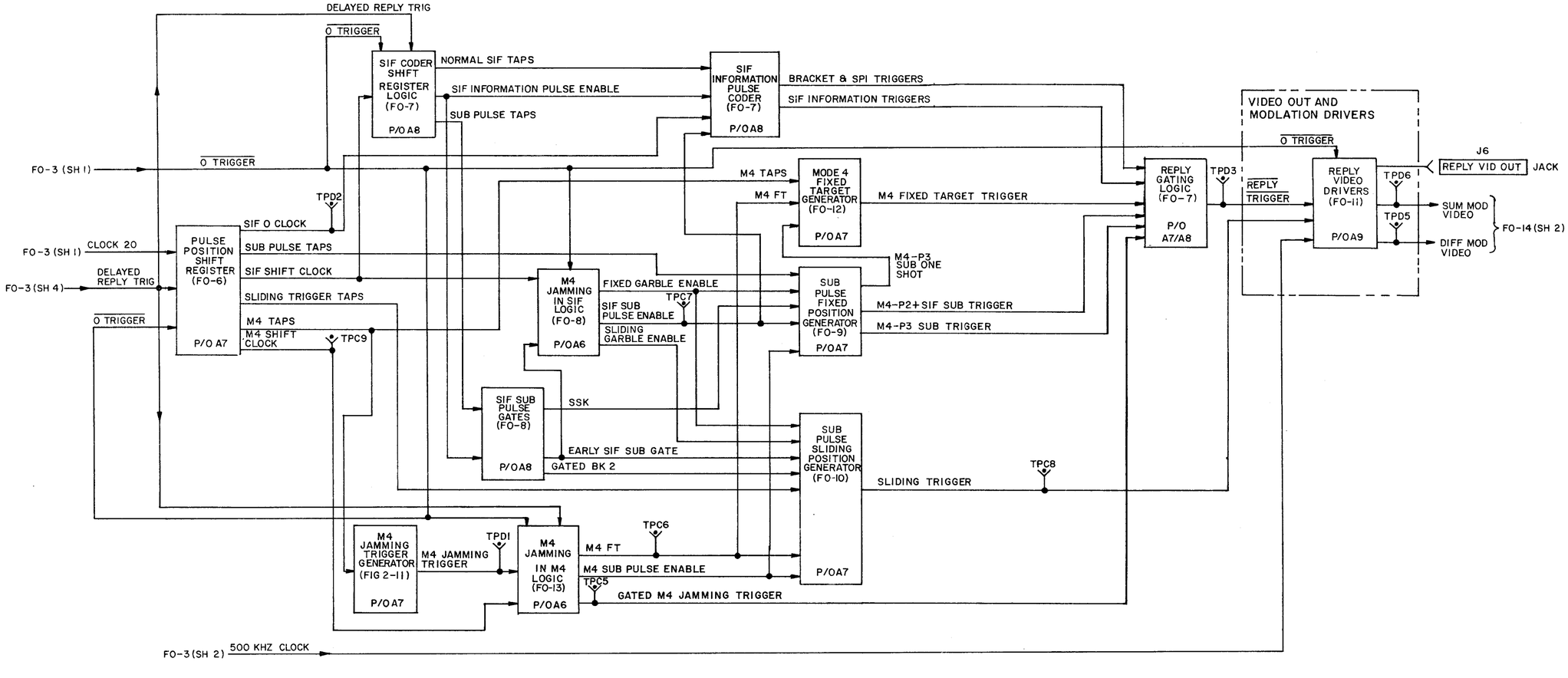
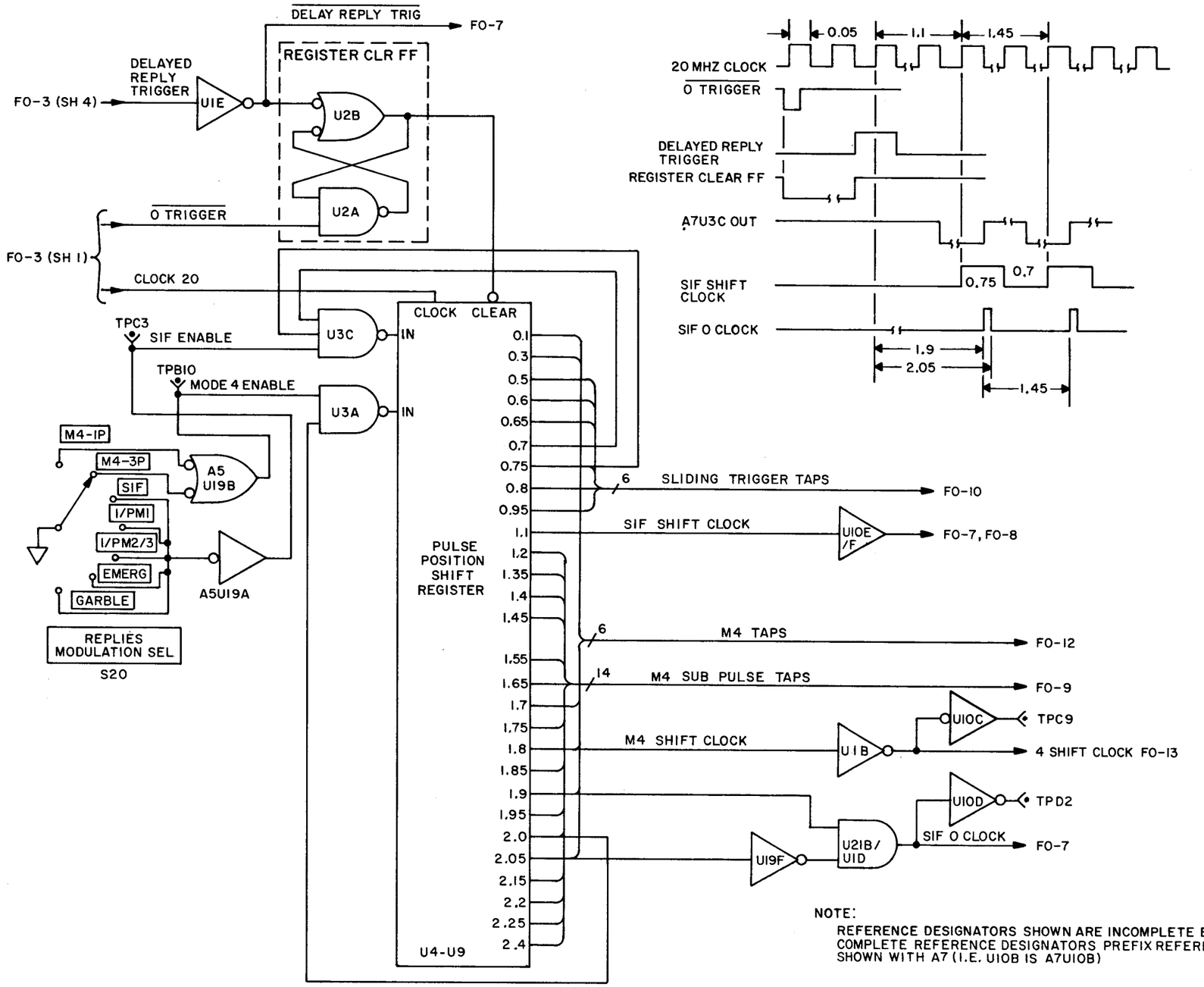


Figure FO-4. Output triggers and mode 4 challenge generator, logic diagram.



EL2UO067

Figure FO-5. SIF and mode 4 reply generator simplified, block diagram.



NOTE:
REFERENCE DESIGNATORS SHOWN ARE INCOMPLETE EXCEPT S20, COMPLETE REFERENCE DESIGNATORS PREFIX REFERENCE DESIGNATOR SHOWN WITH A7 (I.E. U1OB IS A7U1OB)

EL2UO068

Figure FO-6. SIF and mode 4 reply generator pulse position shift register, logic diagram.

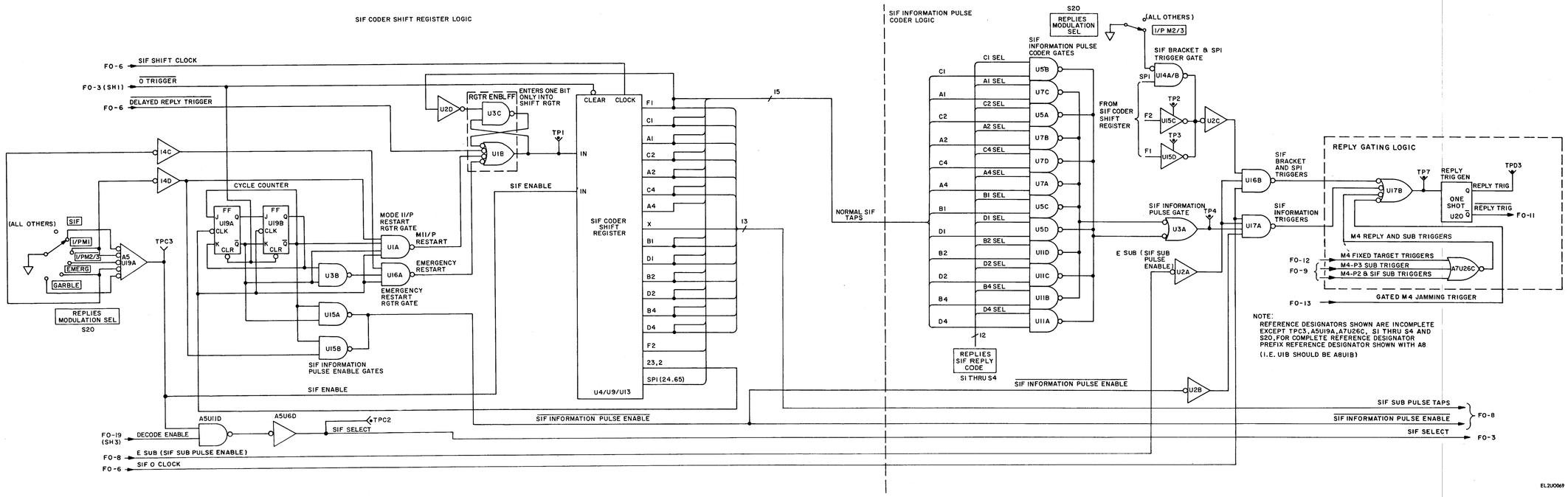


Figure FO-7. SIF and mode 4 reply generator SIF coder, logic diagram.

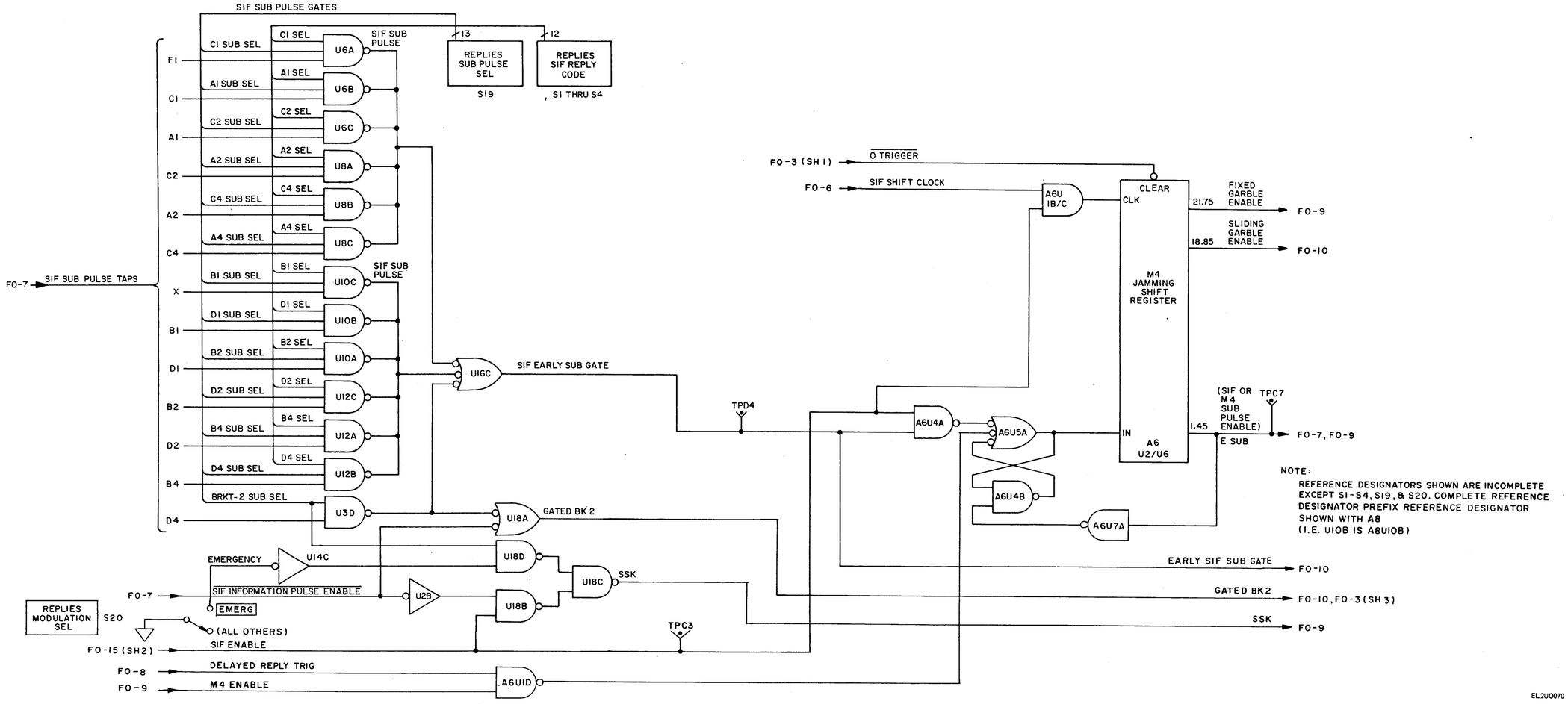


Figure FO-8. SIF and mode 4 reply generator sub pulse gates and M4 jamming in SIF, logic diagram.

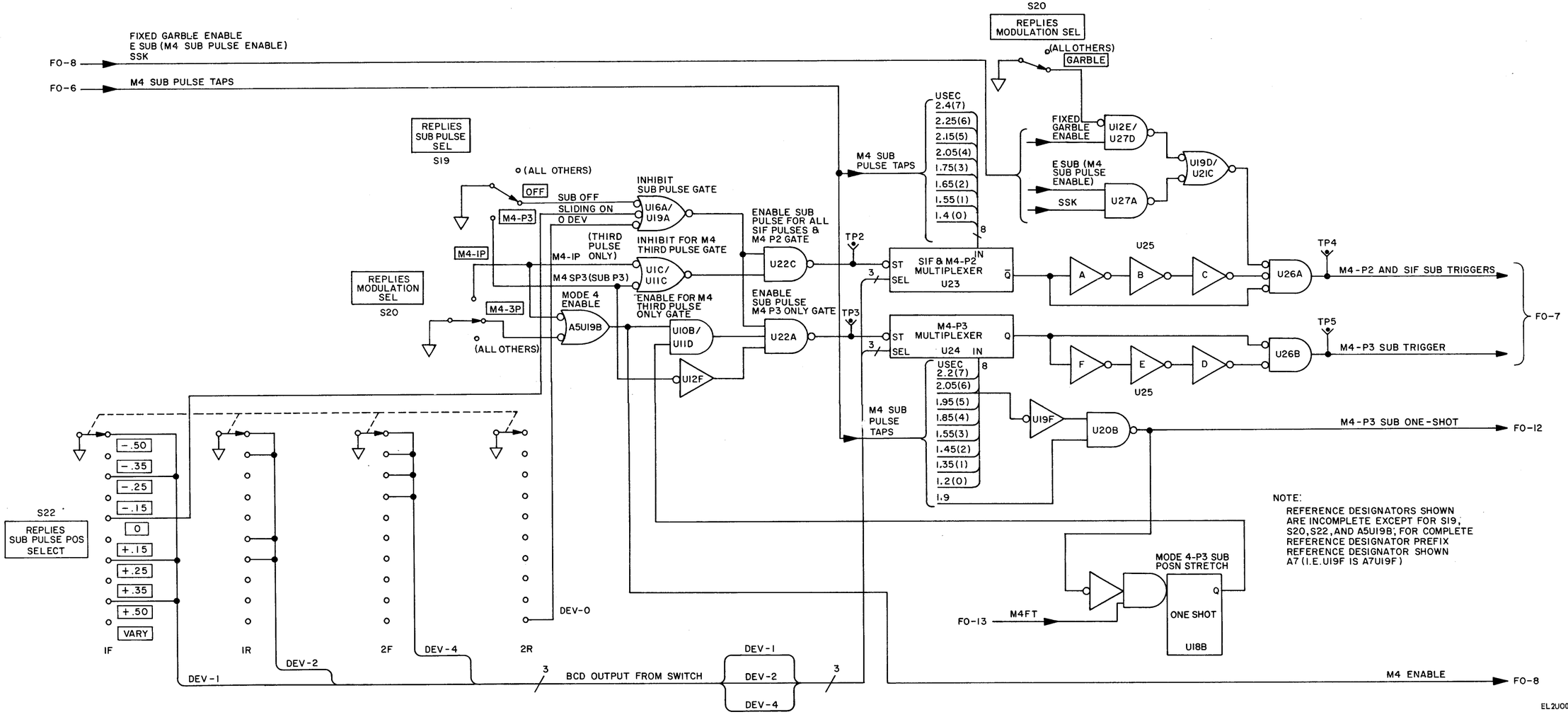
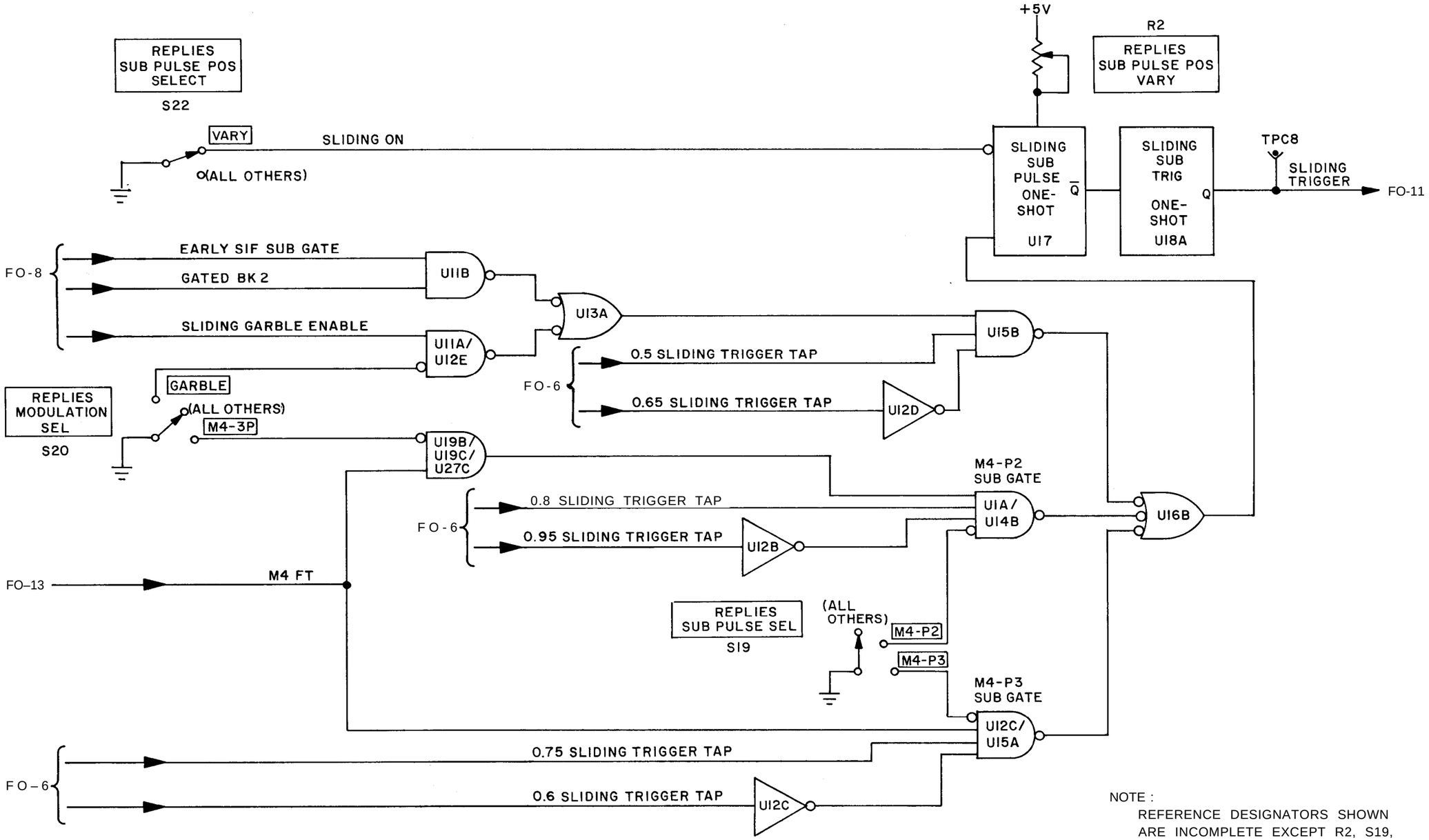


Figure FO-9. SIF and mode 4 reply generator sub pulse fixed position generator, logic diagram.

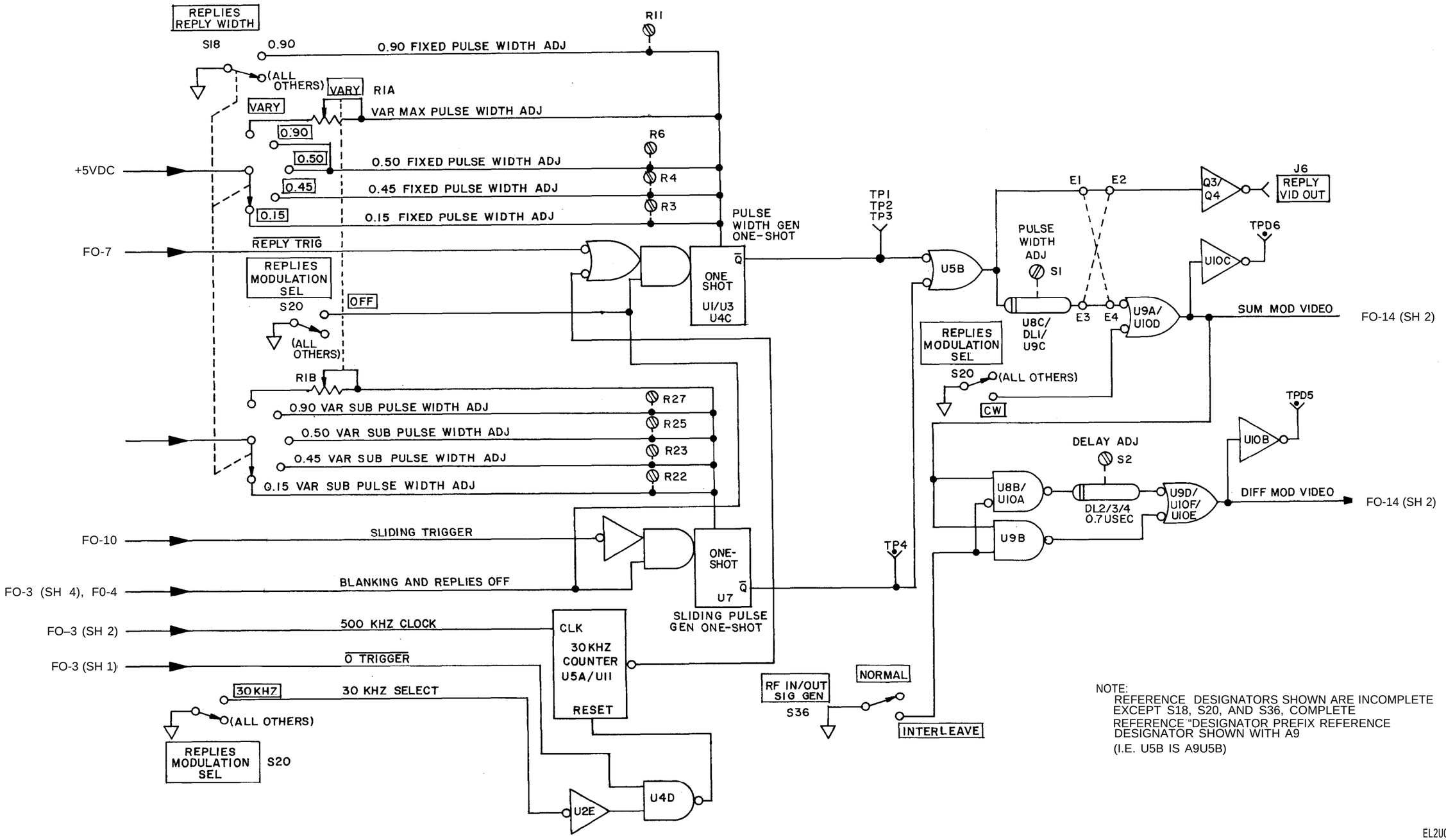


NOTE :
REFERENCE DESIGNATORS SHOWN ARE INCOMPLETE EXCEPT R2, S19, S20 AND S22 ; FOR COMPLETE REFERENCE DESIGNATOR PREFIX REFERENCE DESIGNATOR SHOWN WITH A6

(I.E. U27D IS A6U27D)

EL2UO072

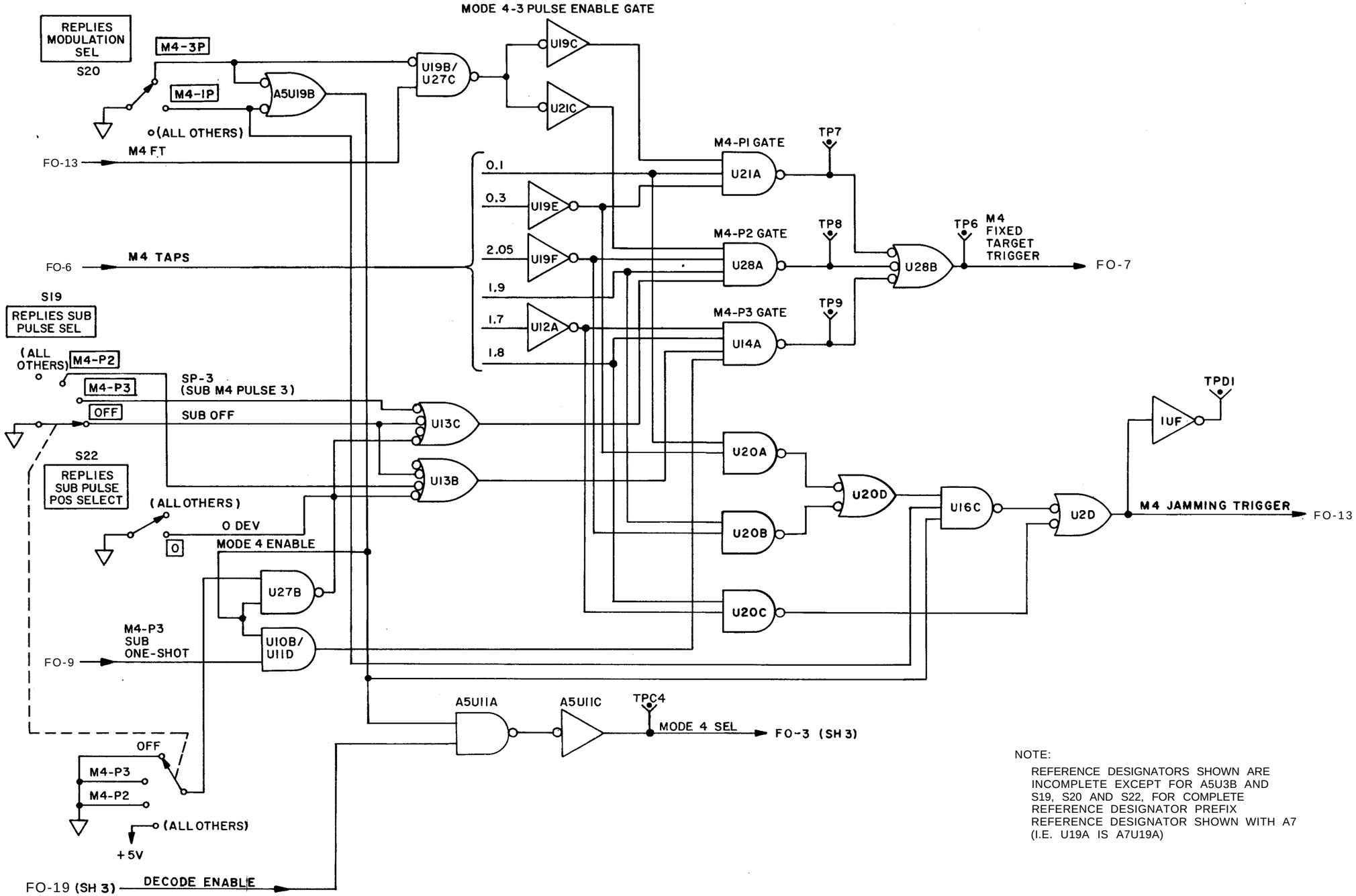
Figure FO–10. SIF and mode 4 reply generator sub pulse sliding position generator, logic diagram.



NOTE:
REFERENCE DESIGNATORS SHOWN ARE INCOMPLETE EXCEPT S18, S20, AND S36, COMPLETE REFERENCE "DESIGNATOR PREFIX REFERENCE DESIGNATOR SHOWN WITH A9
(I.E. U5B IS A9U5B)

EL2U0073

Figure FO-11. SIF and mode 4 reply generator reply video drivers, logic diagram.

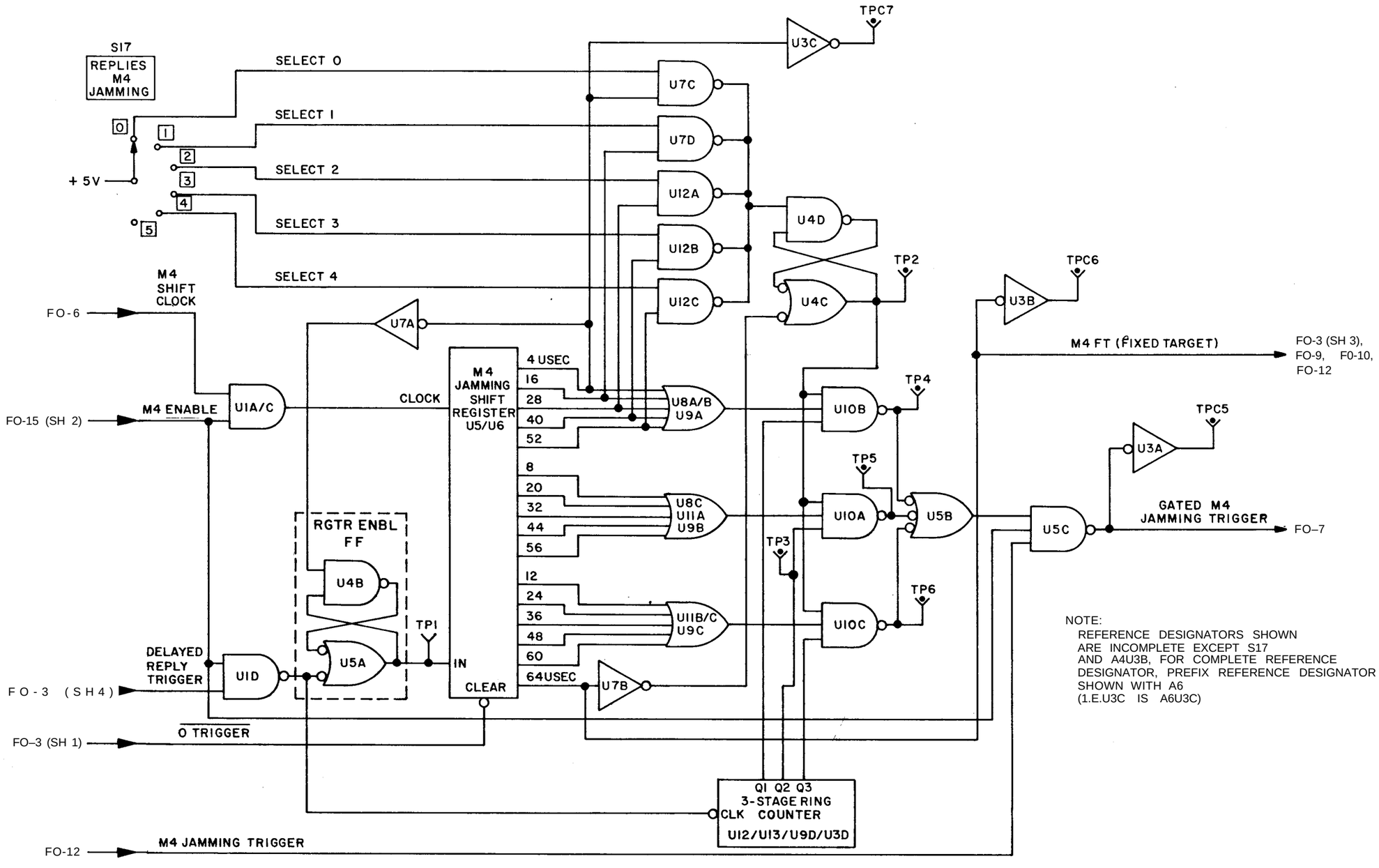


NOTE:

REFERENCE DESIGNATORS SHOWN ARE INCOMPLETE EXCEPT FOR A5U3B AND S19, S20 AND S22, FOR COMPLETE REFERENCE DESIGNATOR PREFIX REFERENCE DESIGNATOR SHOWN WITH A7 (I.E. U19A IS A7U19A)

EL2UO074

Figure FO-12. Mode 4 fixed target generator, logic diagram.



NOTE:
REFERENCE DESIGNATORS SHOWN ARE INCOMPLETE EXCEPT S17 AND A4U3B, FOR COMPLETE REFERENCE DESIGNATOR, PREFIX REFERENCE DESIGNATOR SHOWN WITH A6 (1.E.U3C IS A6U3C)

EL2JO075

Figure FO–13. SIF and mode 4 reply generator M4 jamming in mode 4, logic diagram.

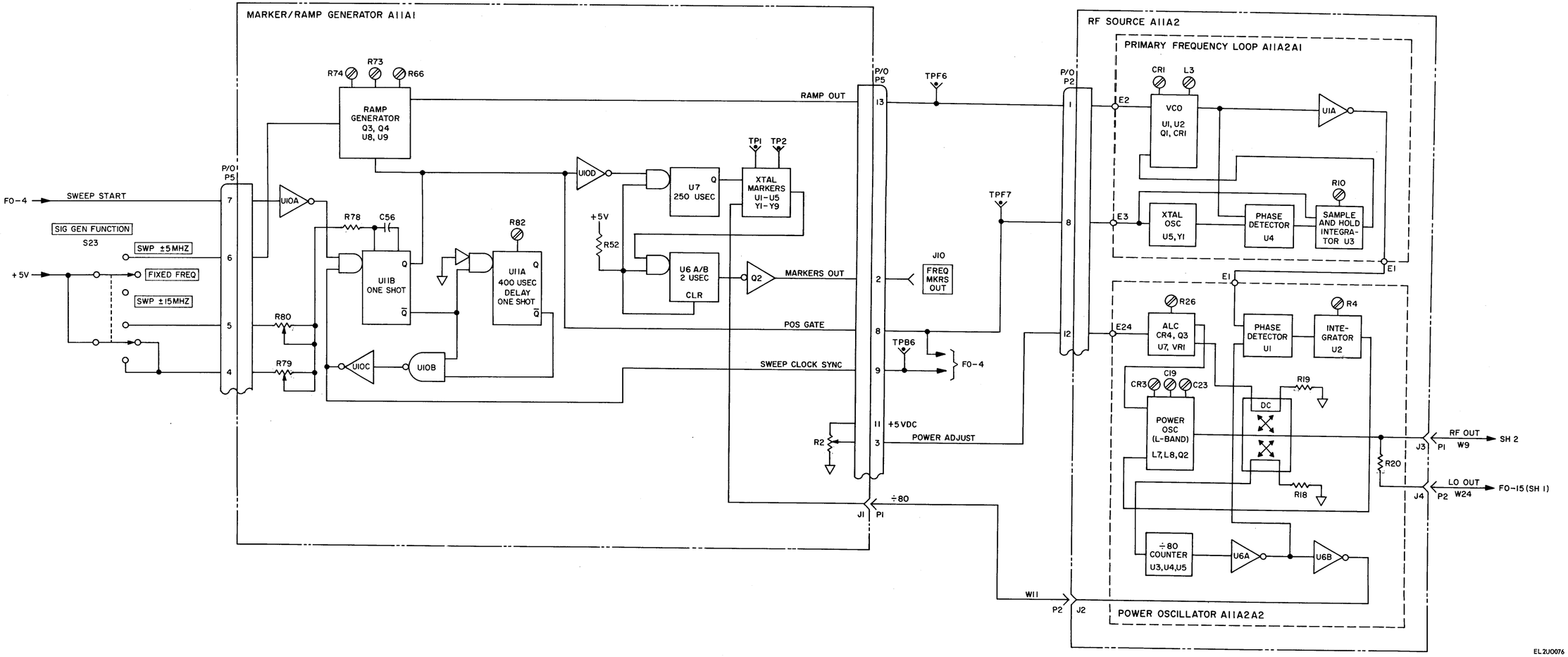
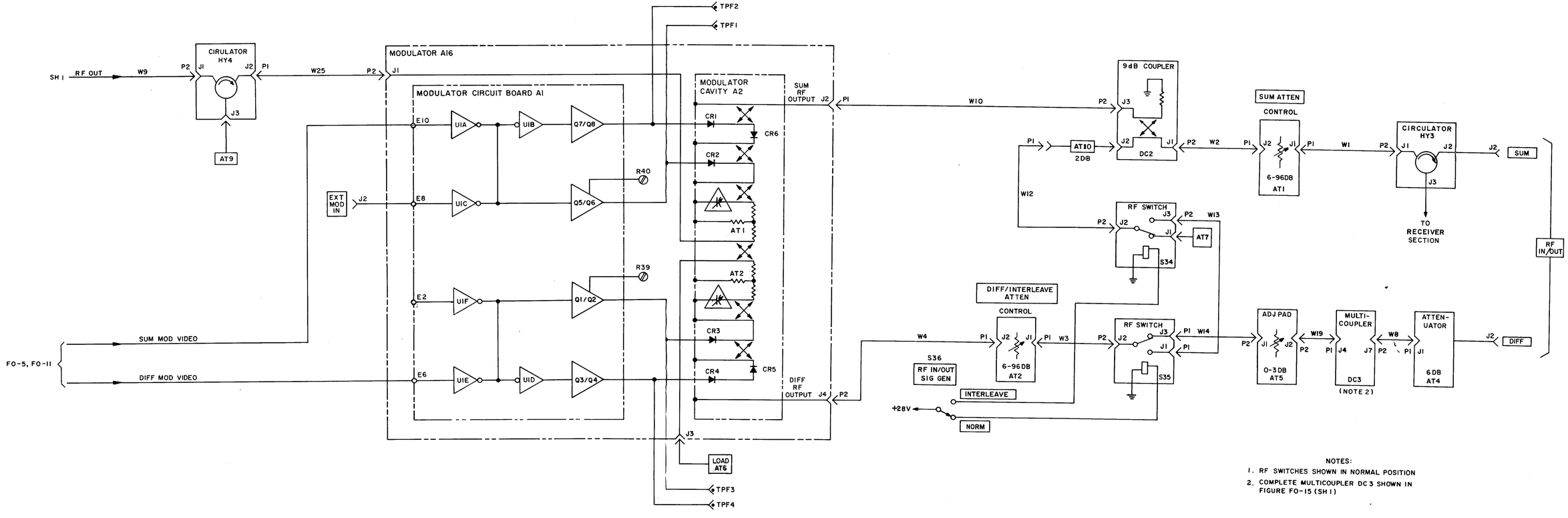


Figure FO-14. Rf signal generator, block diagram (sheet 1 of 2).



NOTES:

1. RF SWITCHES SHOWN IN NORMAL POSITION
2. COMPLETE MULTICOUPLER DC 3 SHOWN IN FIGURE FO-15 (SH 1)

EL2U0077

Figure FO-14. Rf signal generator, block diagram (sheet 2 of 2).

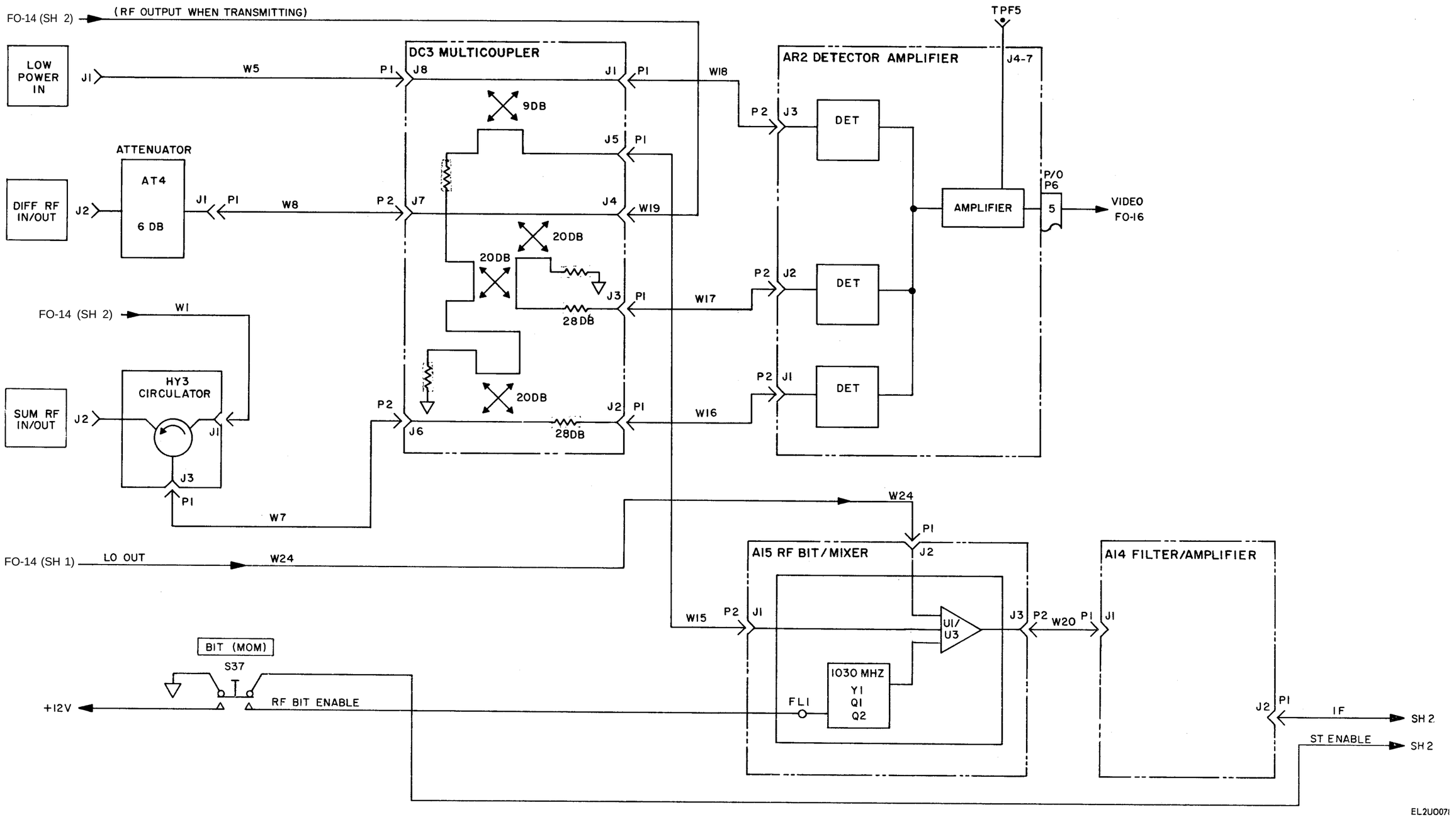


Figure FO-15. Receiver block diagram (sheet 1 of 2).

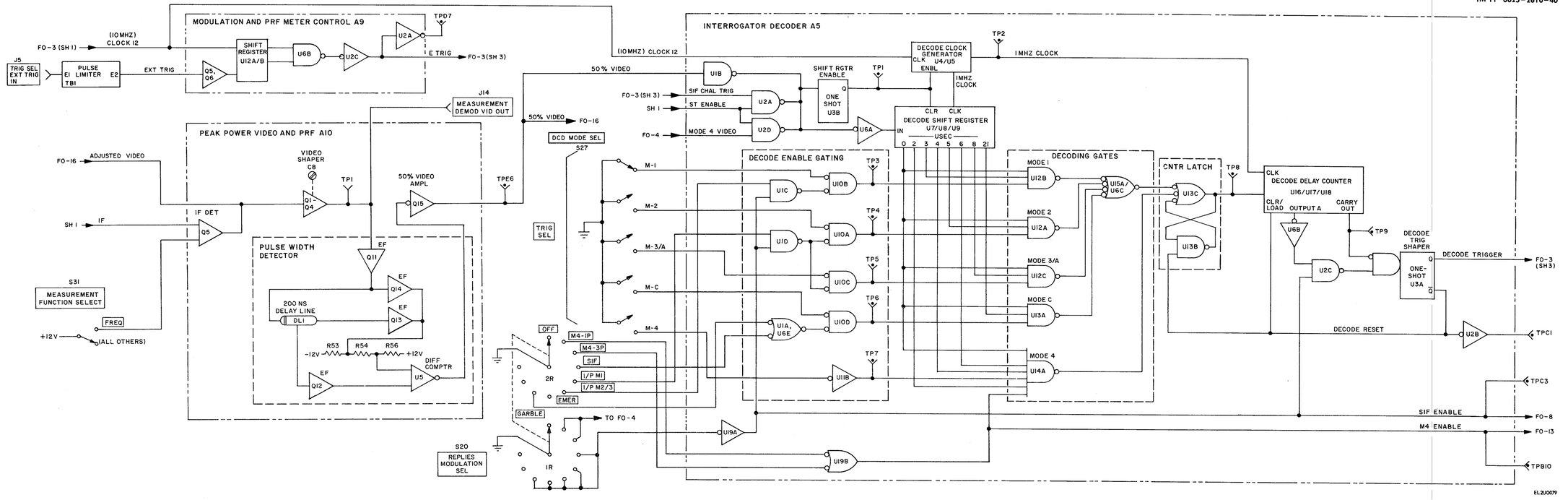


Figure FO-15. Receiver block diagram (sheet 2 of 2).

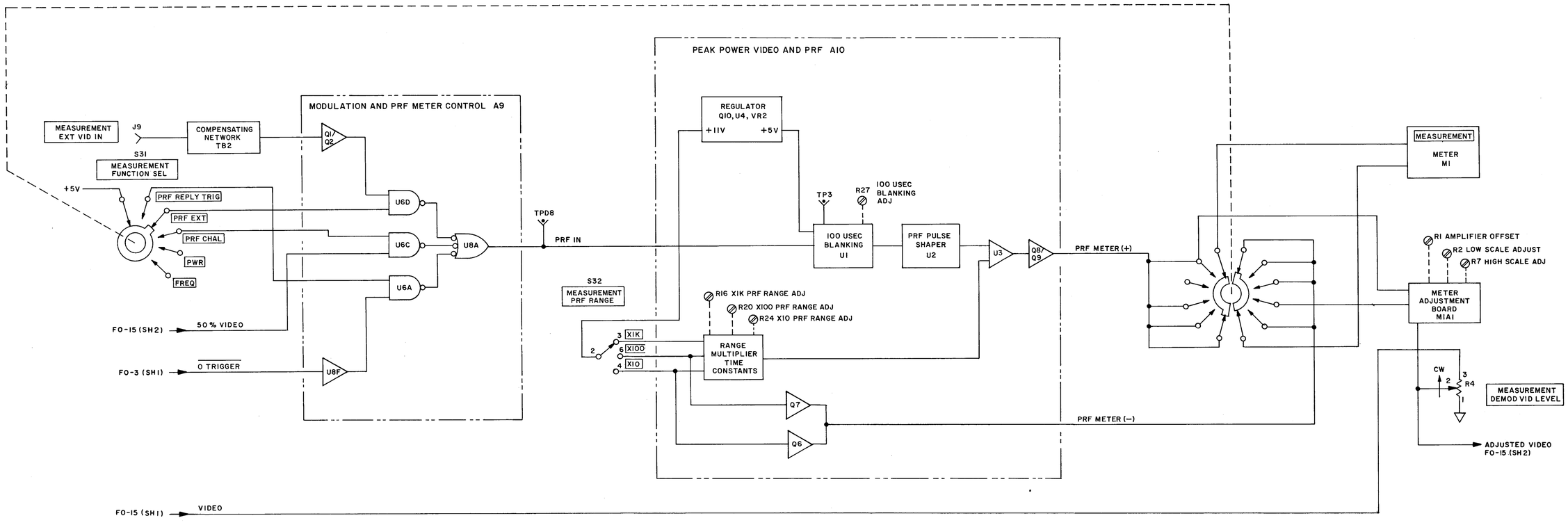
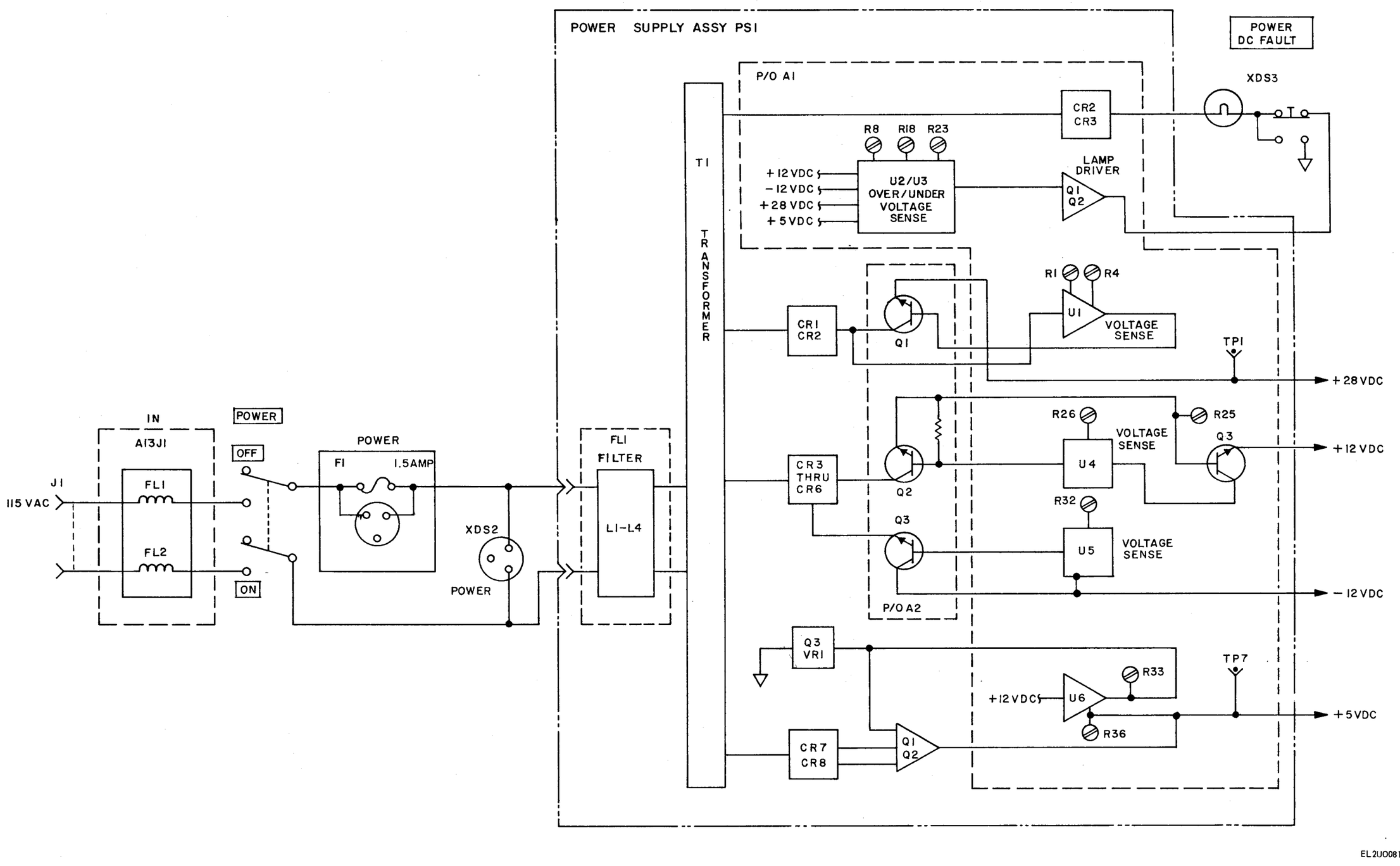


Figure FO-16. Measurement section, logic diagram.



EL2UO081

Figure FO–17. Power Supply block diagram.

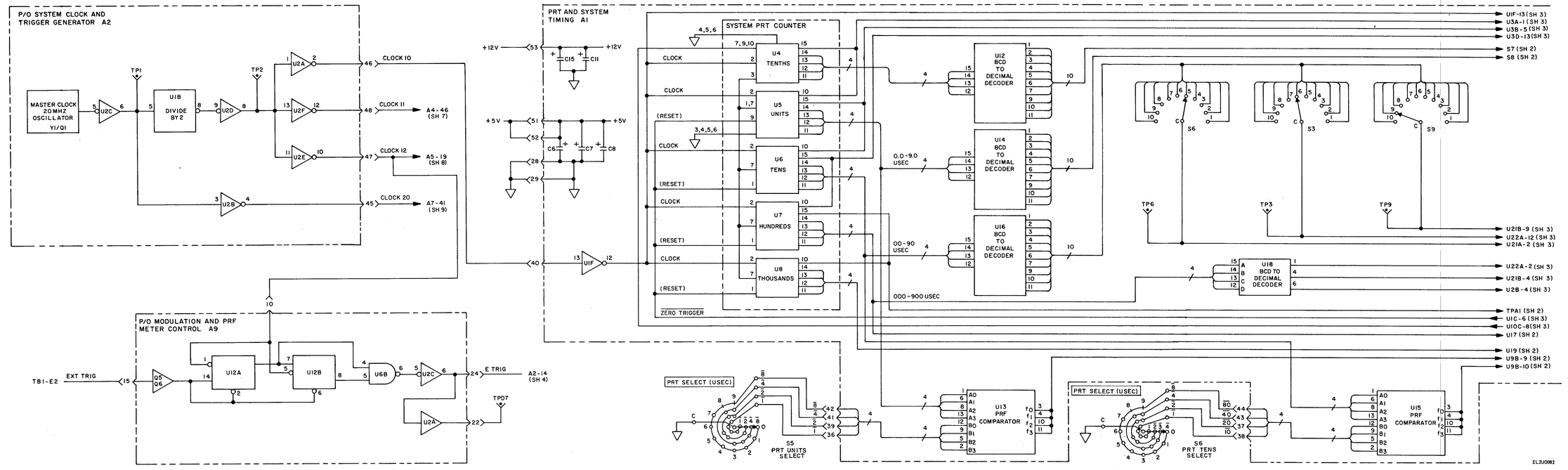


Figure FO-18. Troubleshooting, logic diagram (sheet 1 of 15).

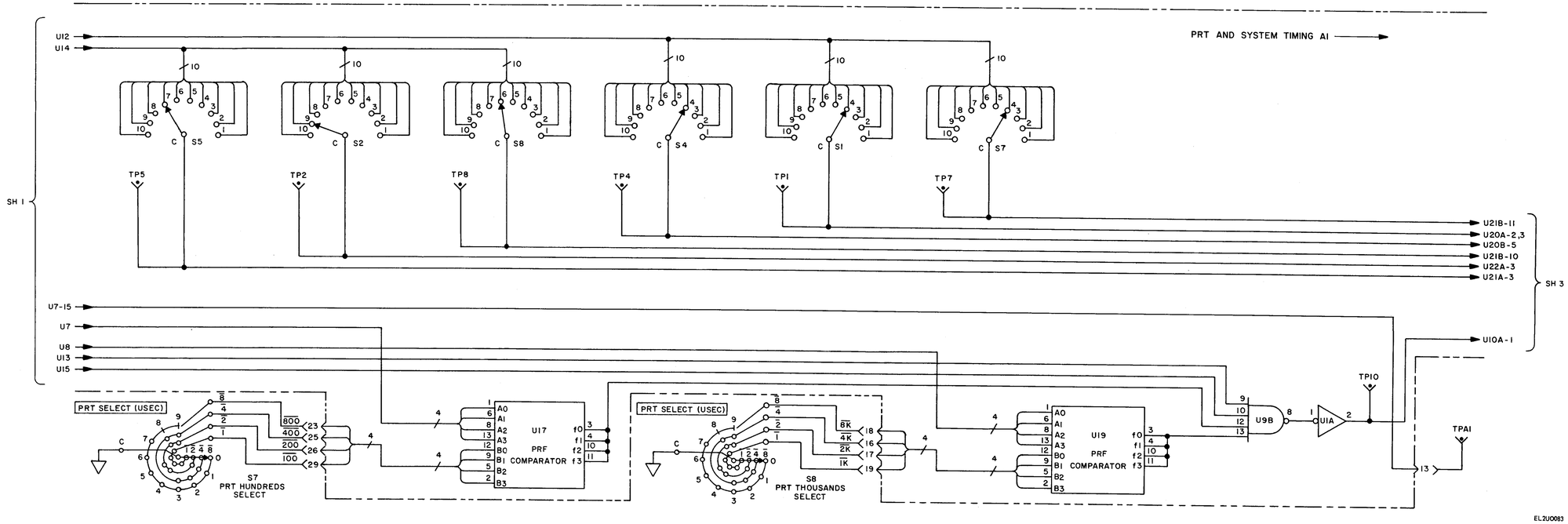


Figure FO-18. Troubleshooting, logic diagram (sheet 2 of 15).

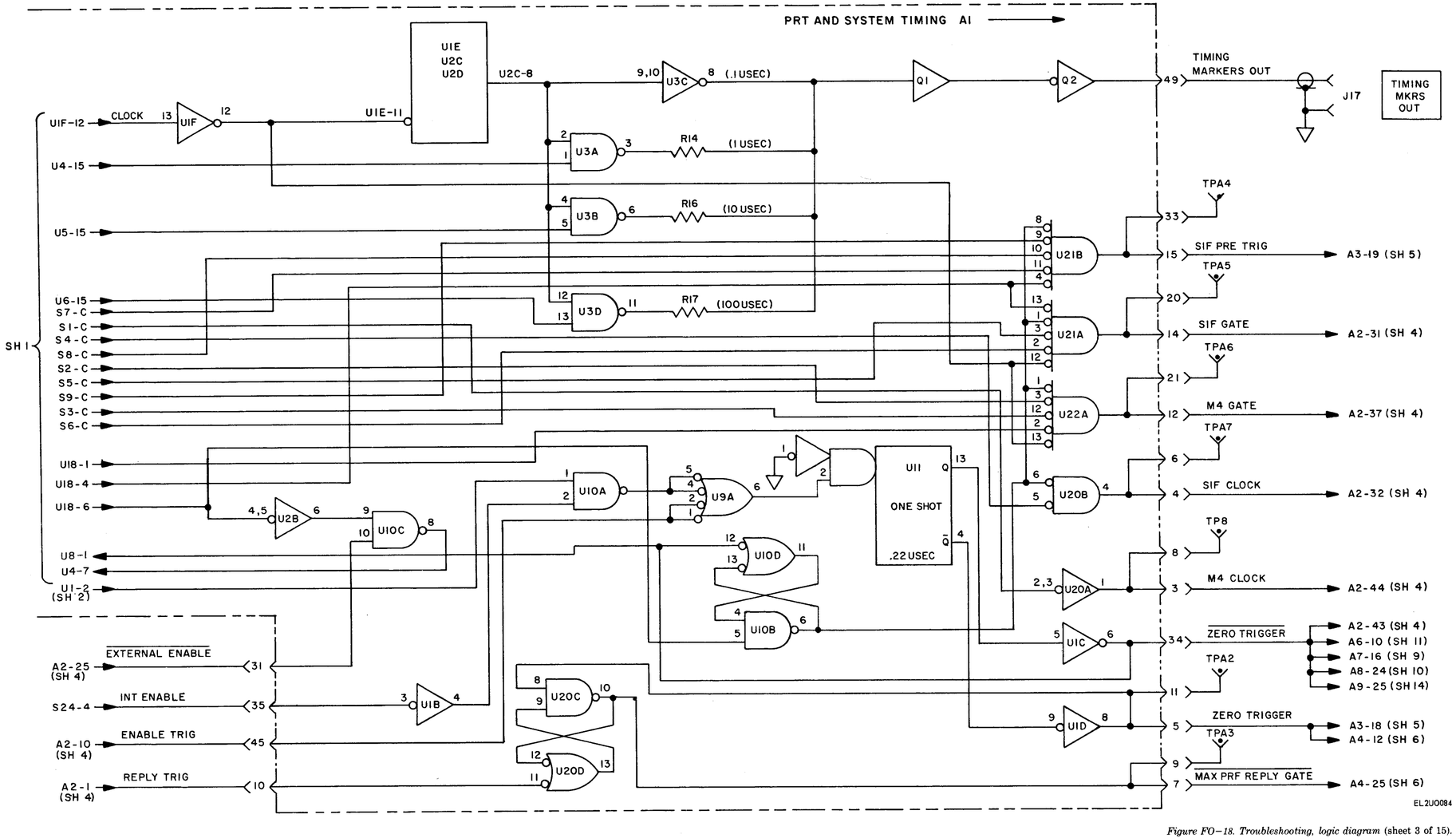


Figure FO-18. Troubleshooting, logic diagram (sheet 3 of 15).

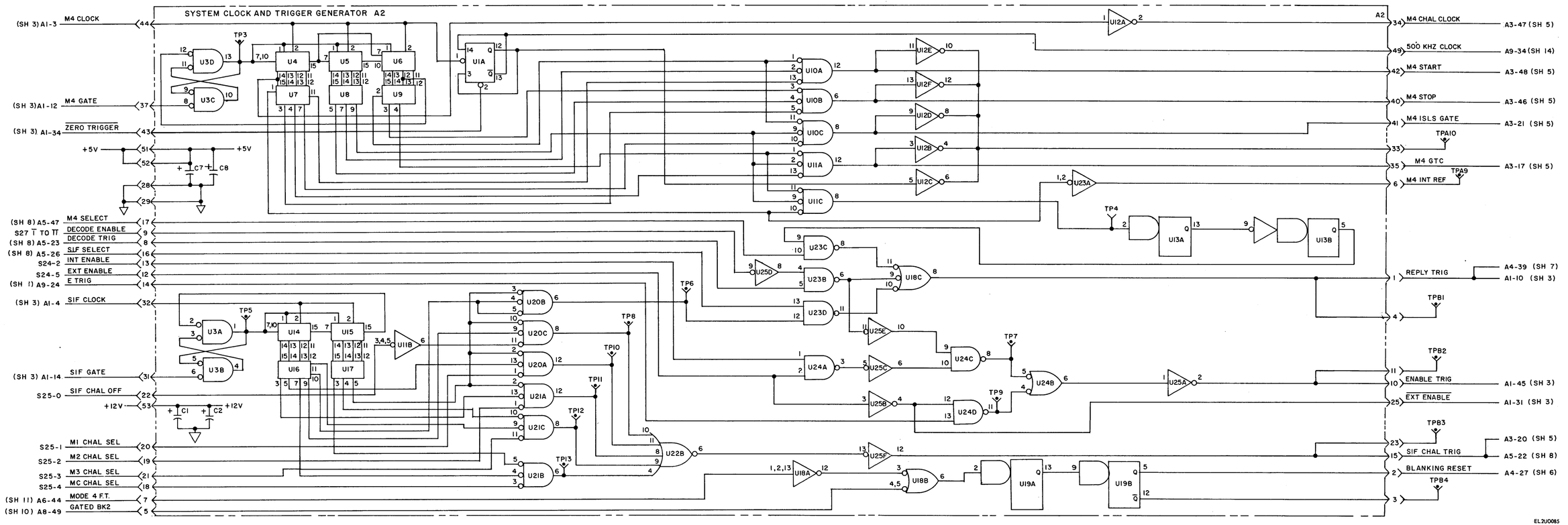


Figure FO-18. Troubleshooting, logic diagram (sheet 4 of 15).

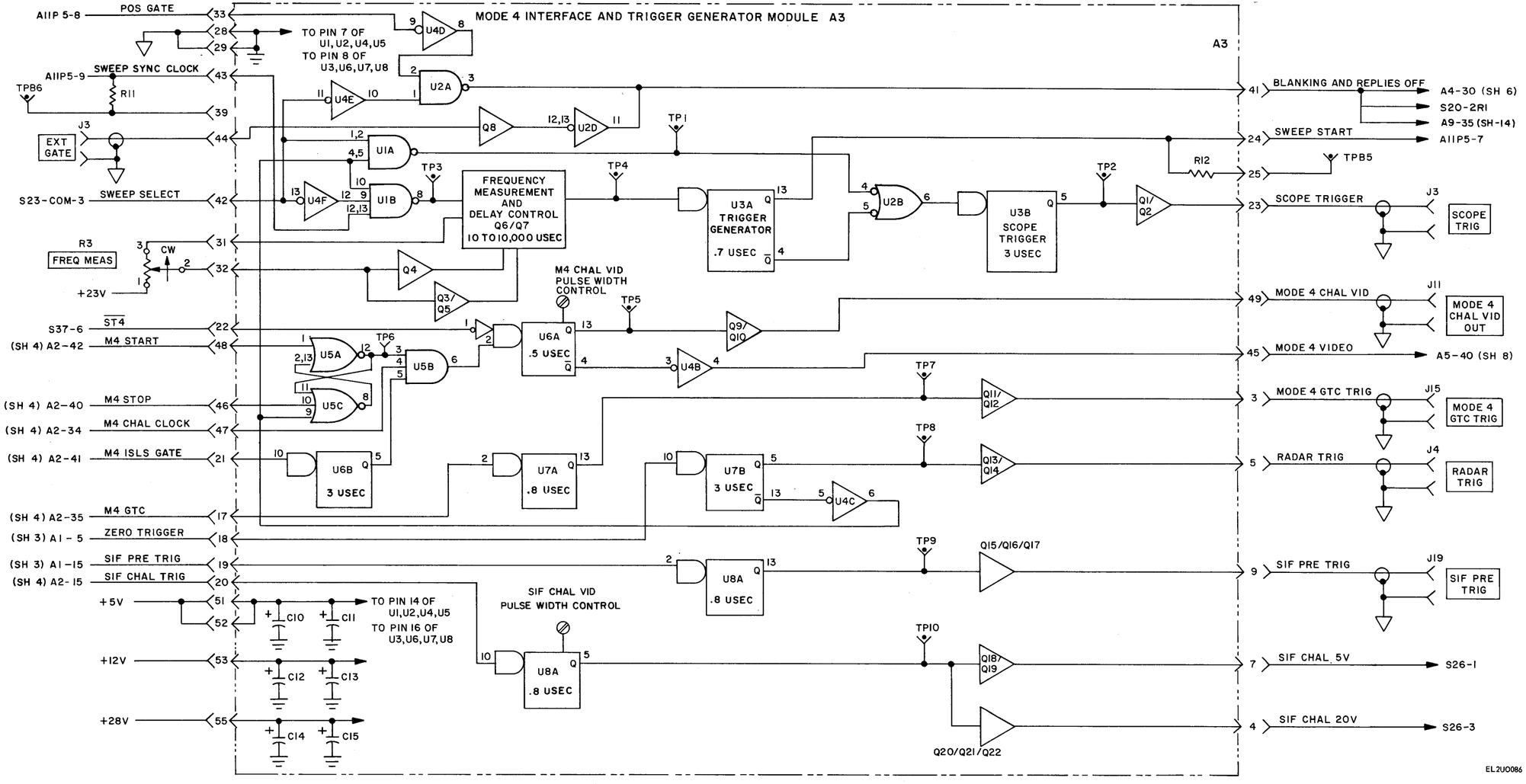
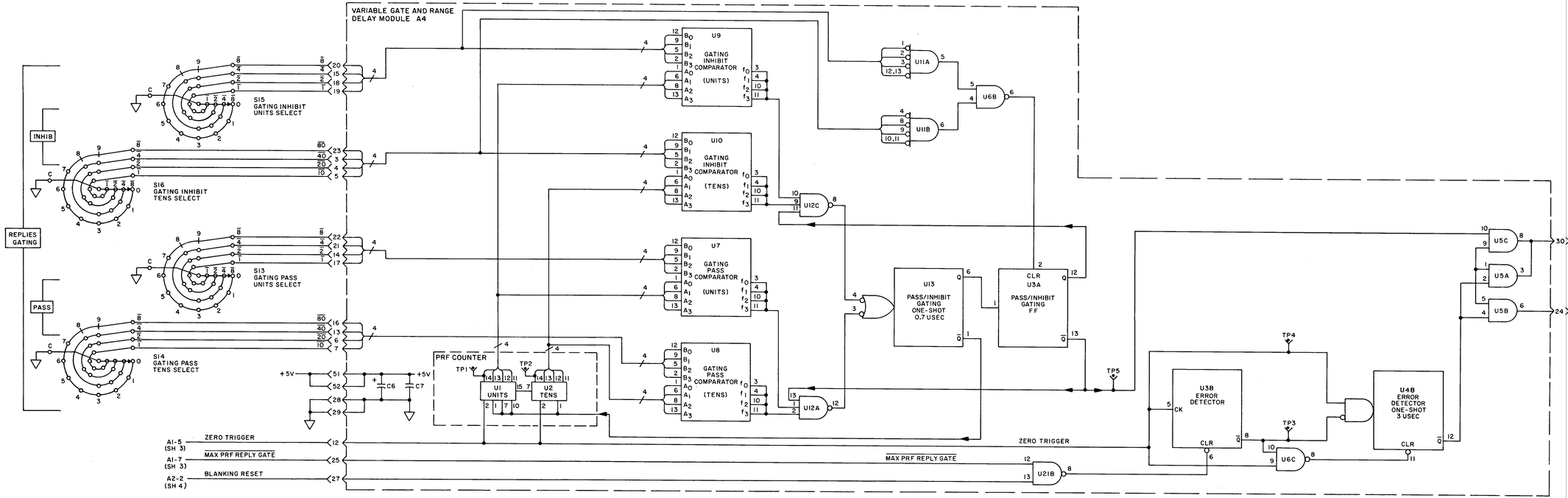
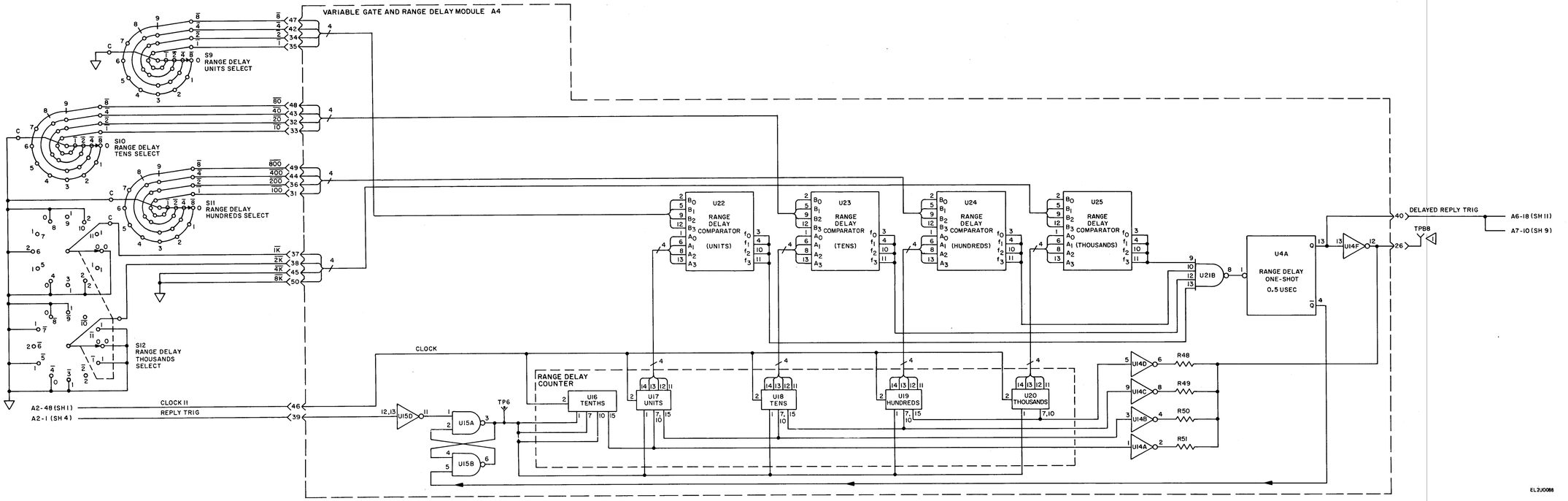


Figure FO-18. Troubleshooting, logic diagram (sheet 5 of 15).



EL2JO087

Figure FO-18. Troubleshooting, logic diagram (sheet 6 of 15).



EL2J0088

Figure FO-18. Troubleshooting, logic diagram (sheet 7 of 15).

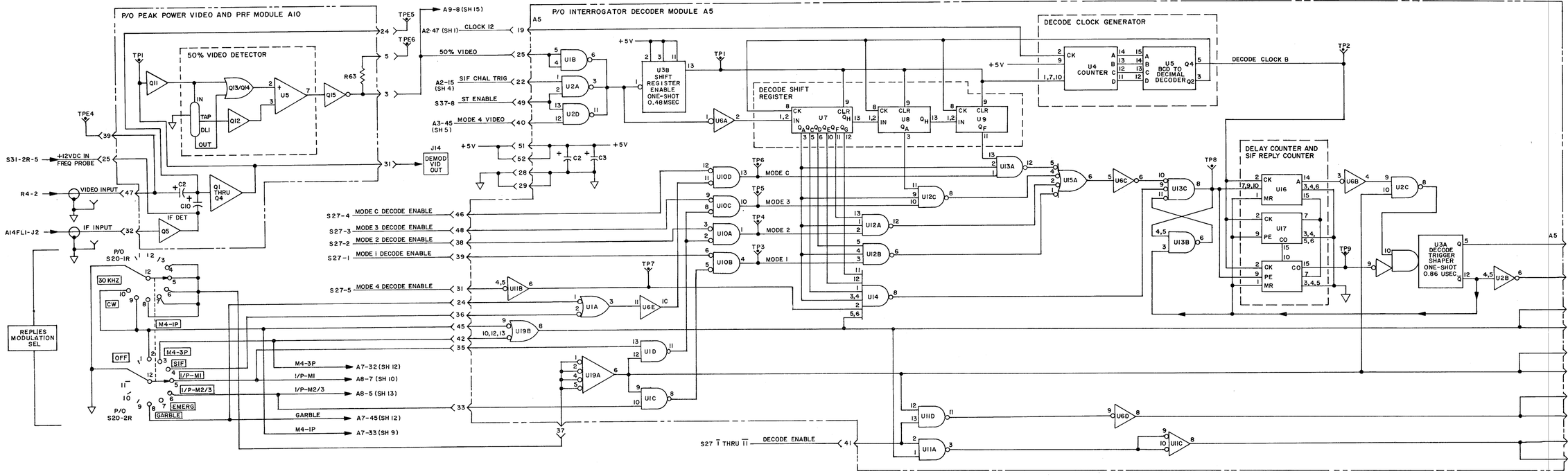
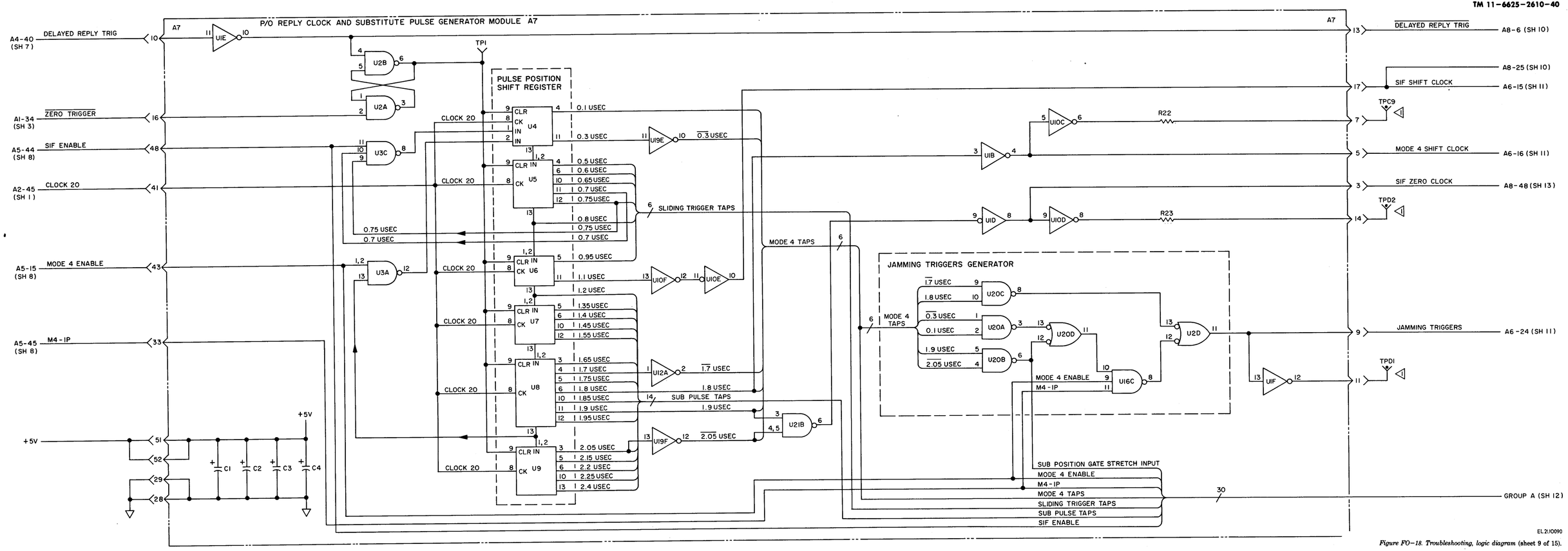


Figure FO-18. Troubleshooting, logic diagram (sheet 8 of 15).



EL21I0090

Figure FO-18. Troubleshooting, logic diagram (sheet 9 of 15).

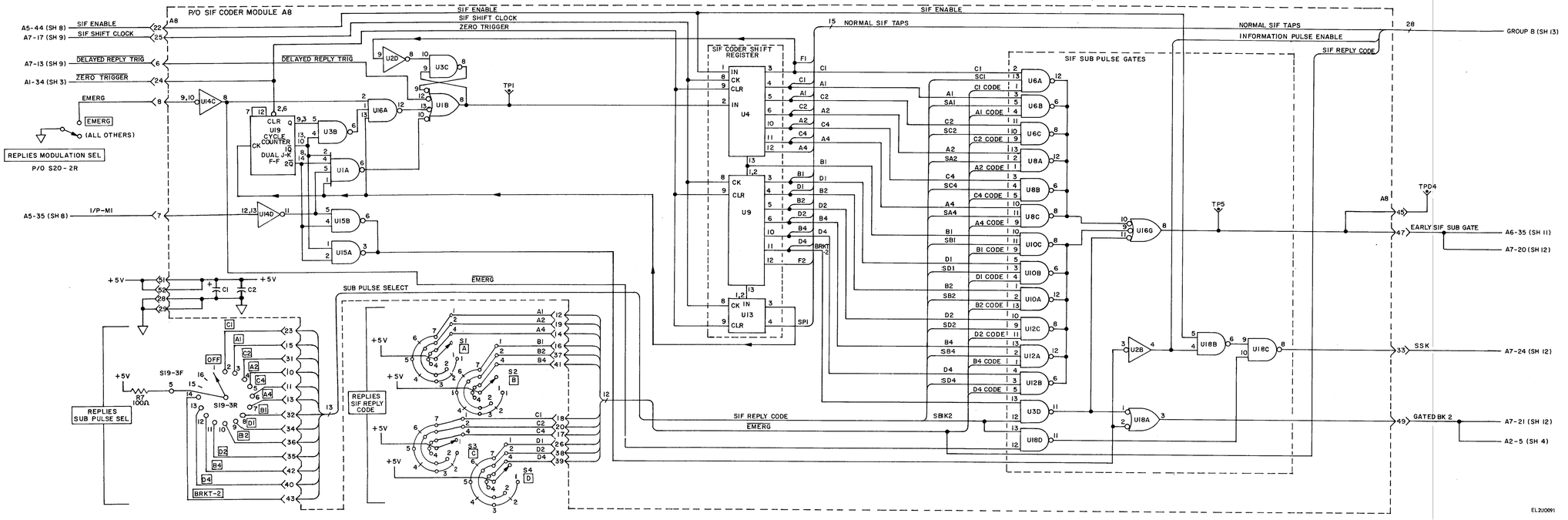


Figure FO-18. Troubleshooting, logic diagram (sheet 10 of 15).

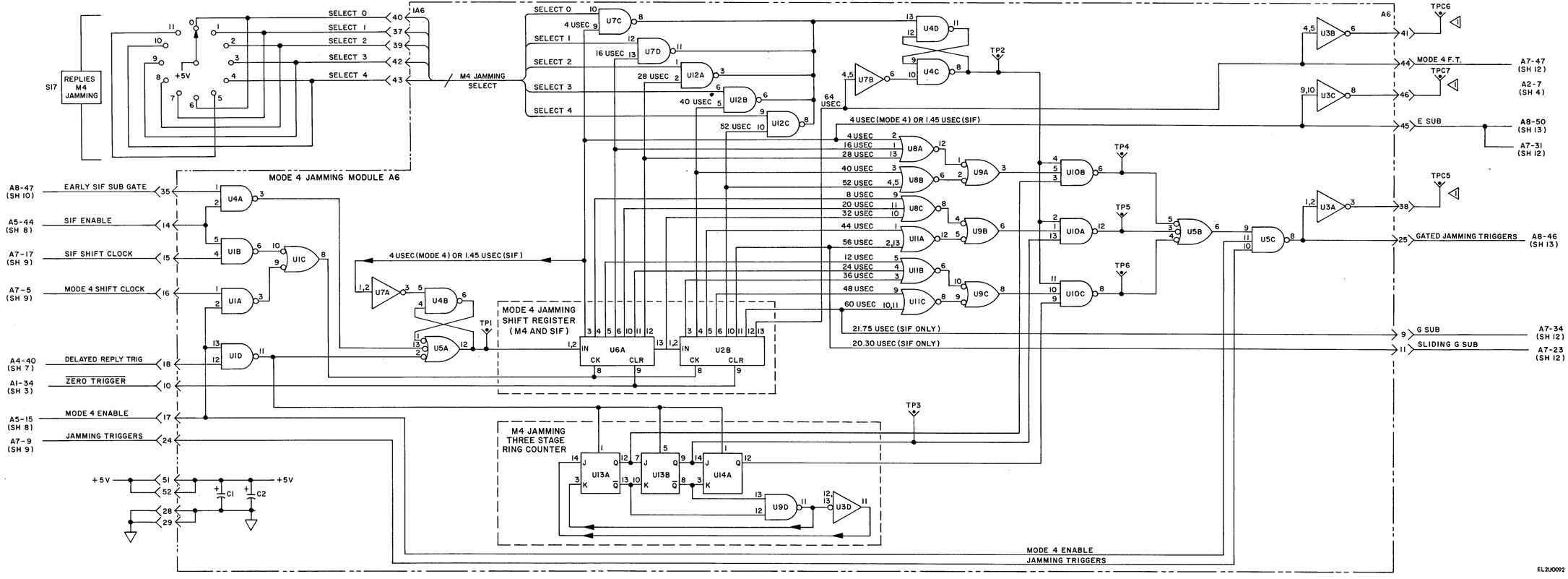
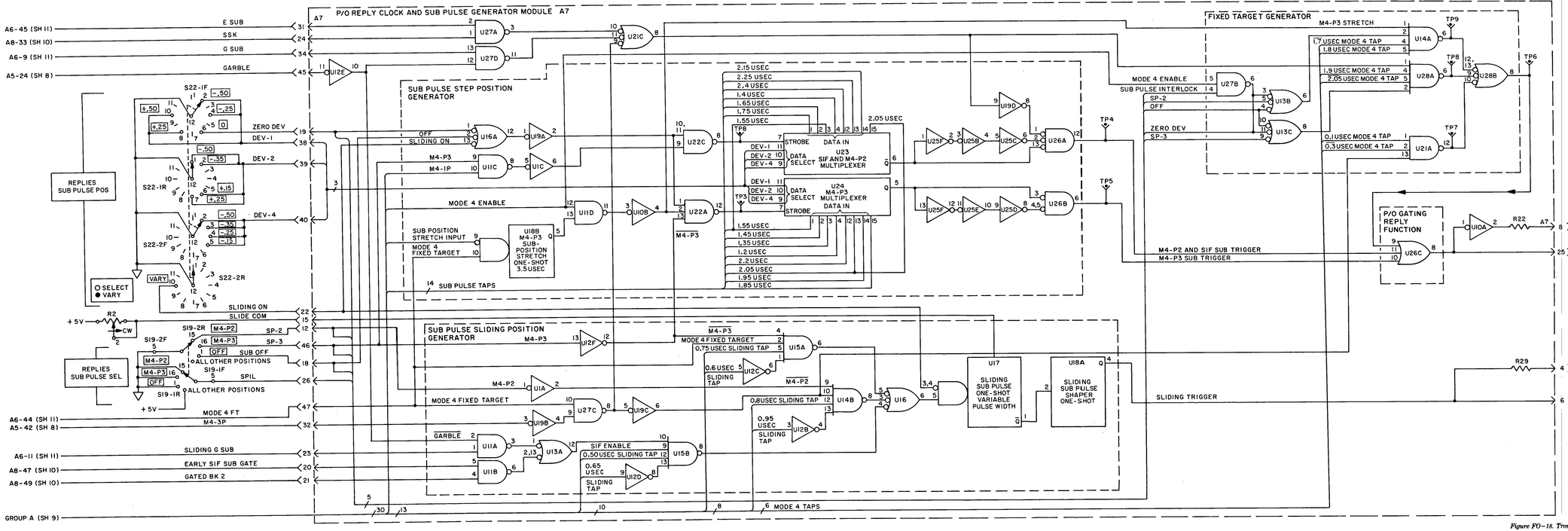


Figure FO-18. Troubleshooting, logic diagram (sheet 11 of 15).



EL2UD093

Figure FO-18. Troubleshooting, logic diagram (sheet 12 of 15).

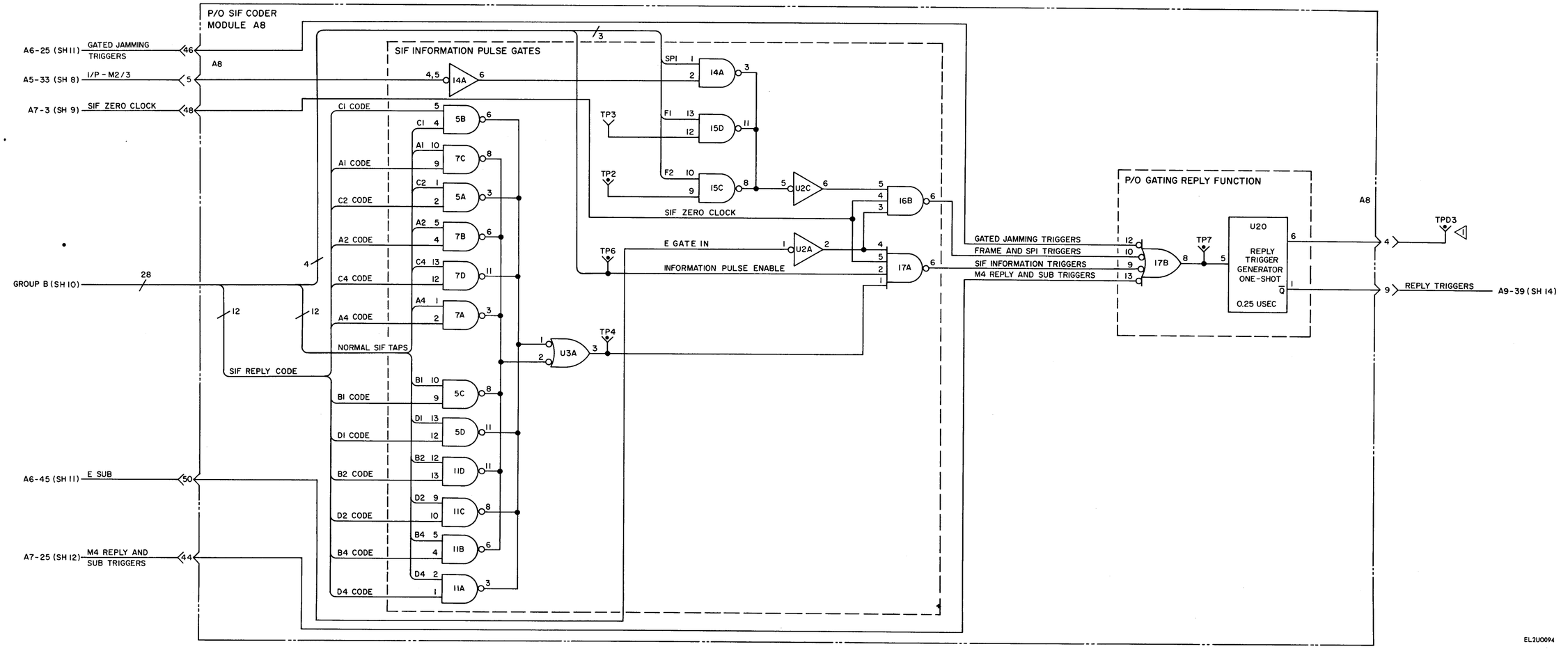


Figure FO-18. Troubleshooting, logic diagram (sheet 13 of 15).

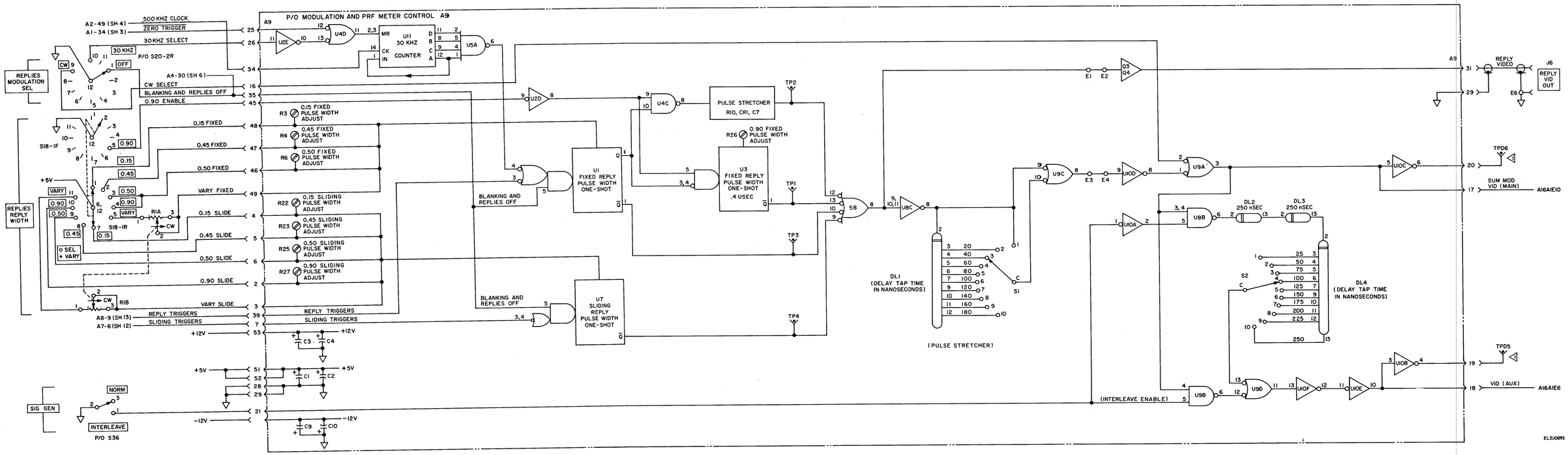
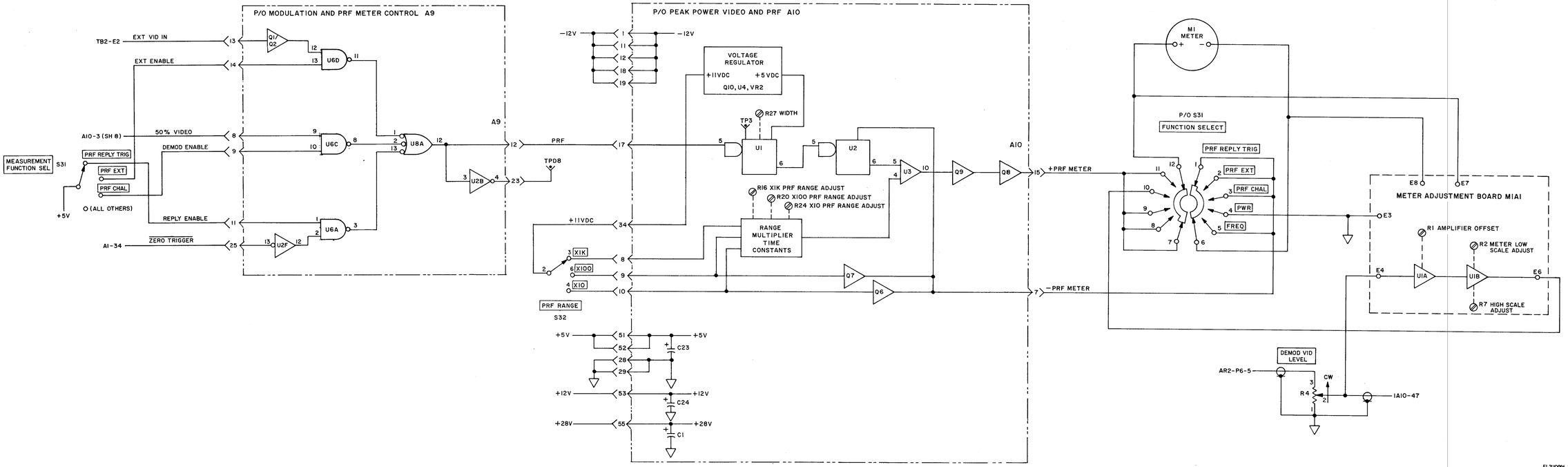
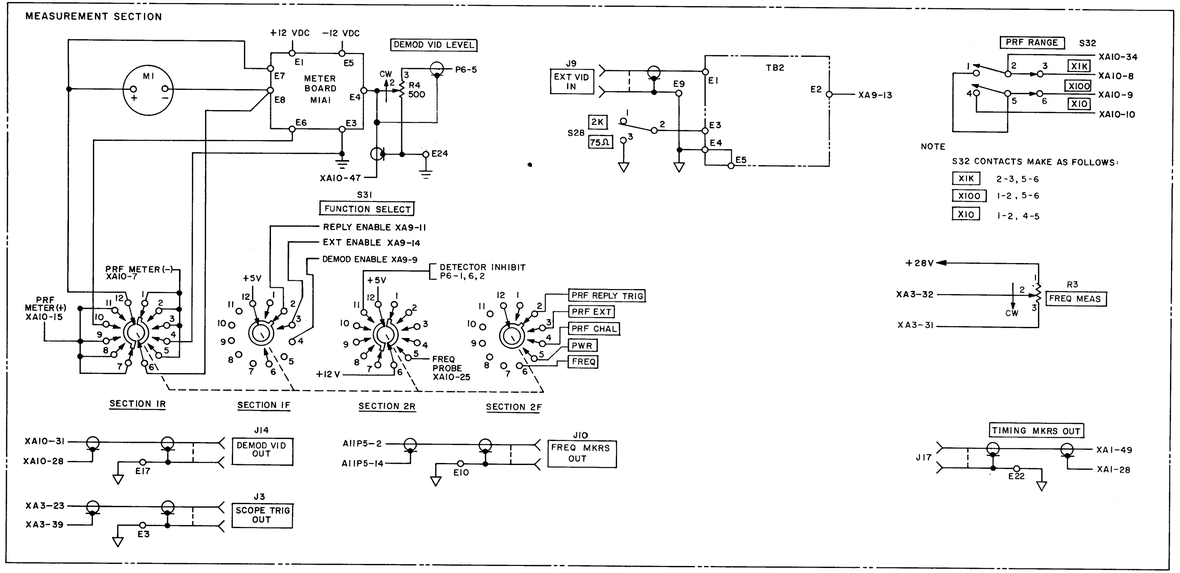


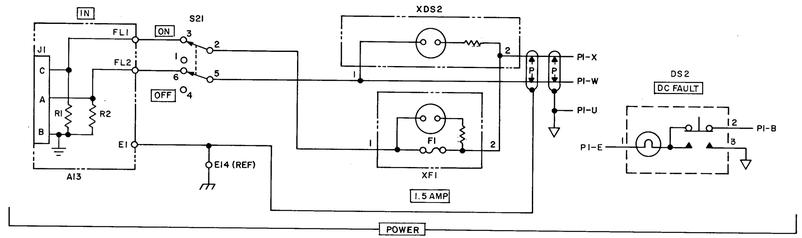
Figure FO-18. Troubleshooting, logic diagram (sheet 14 of 15).

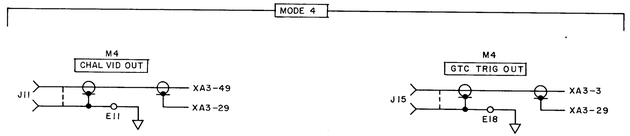


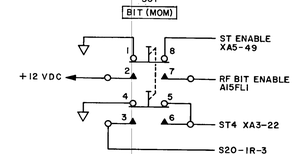
EL2JU096

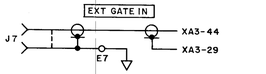
Figure FO-18. Troubleshooting, logic diagram (sheet 15 of 15).

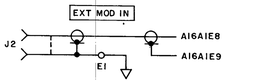






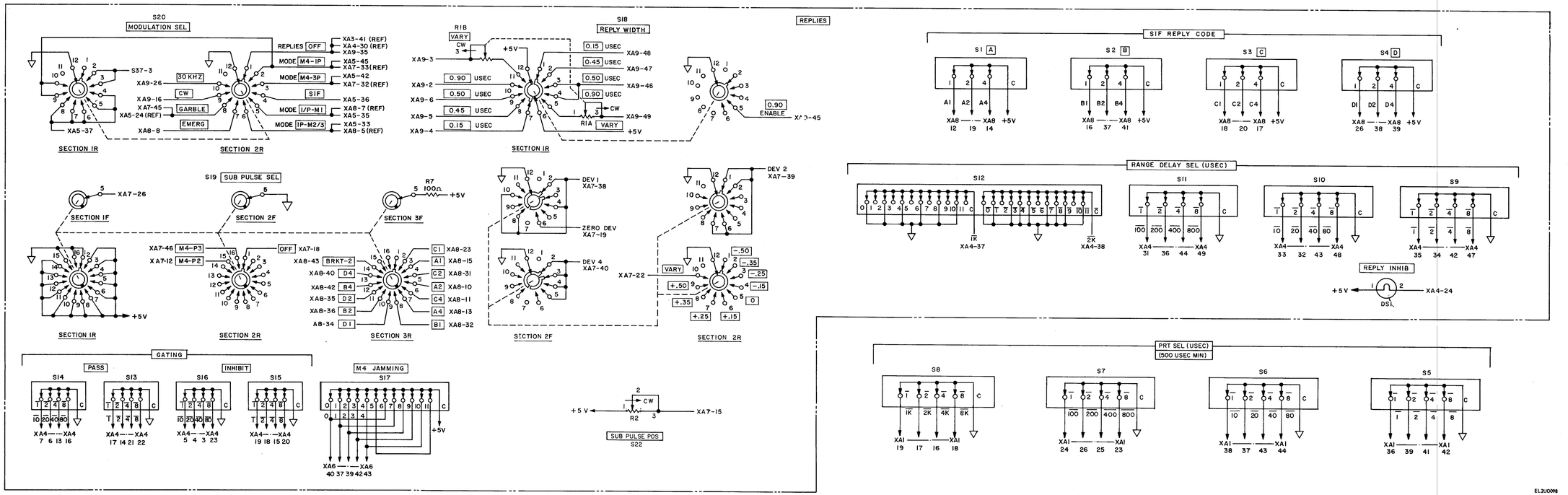






EL2U0097

Figure FO-19. Test set, schematic diagram (sheet 1 of 6).



EL2UO098

Figure FO-19. Test set, schematic diagram (sheet 2 of 6).

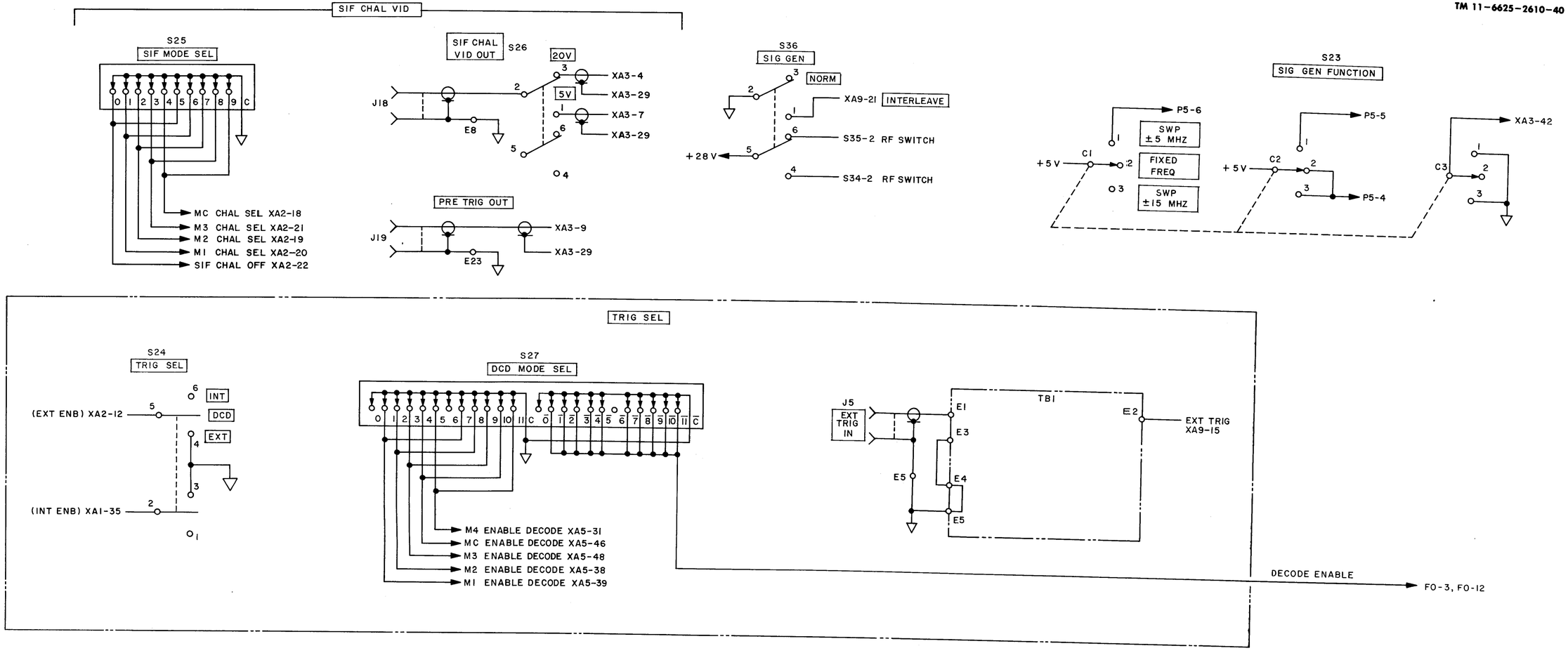


Figure FO-19. Test set, schematic diagram (sheet 3 of 6).

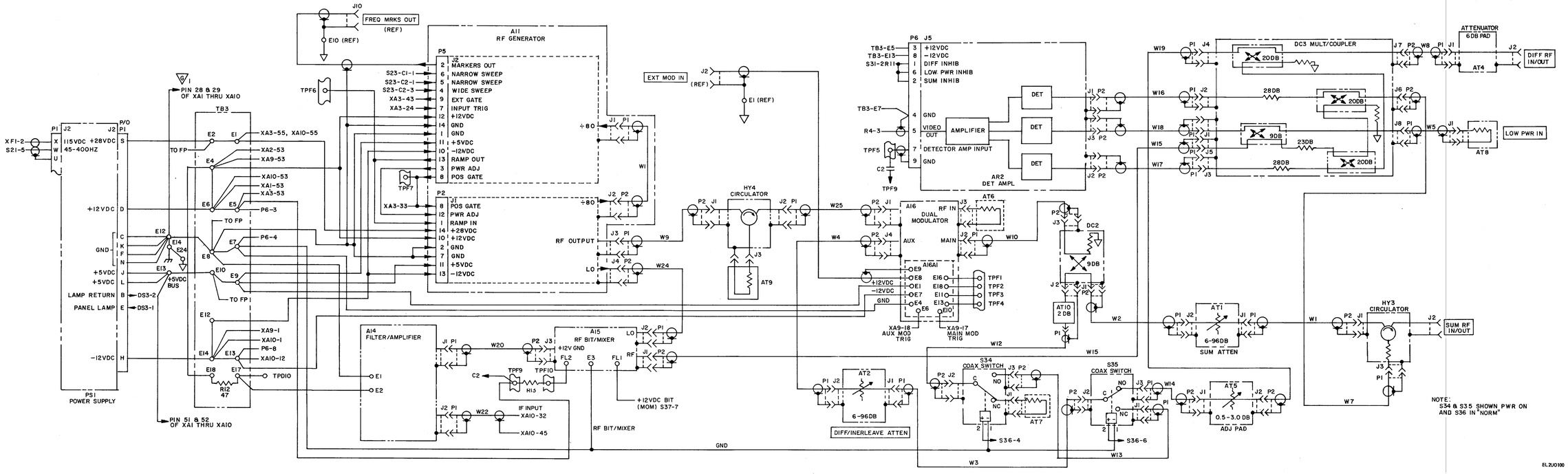


Figure FO-19. Test set, schematic diagram (sheet 4 of 6).

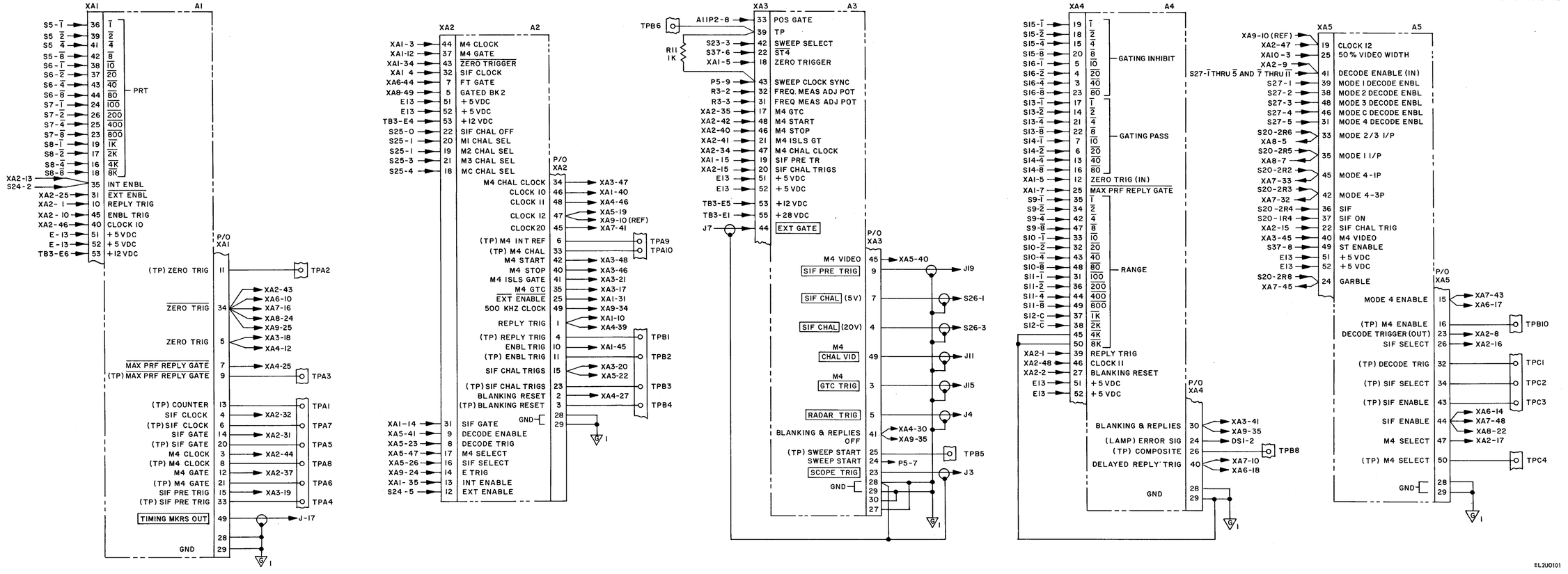


Figure FO-19. Test set, schematic diagram (sheet 5 of 6).

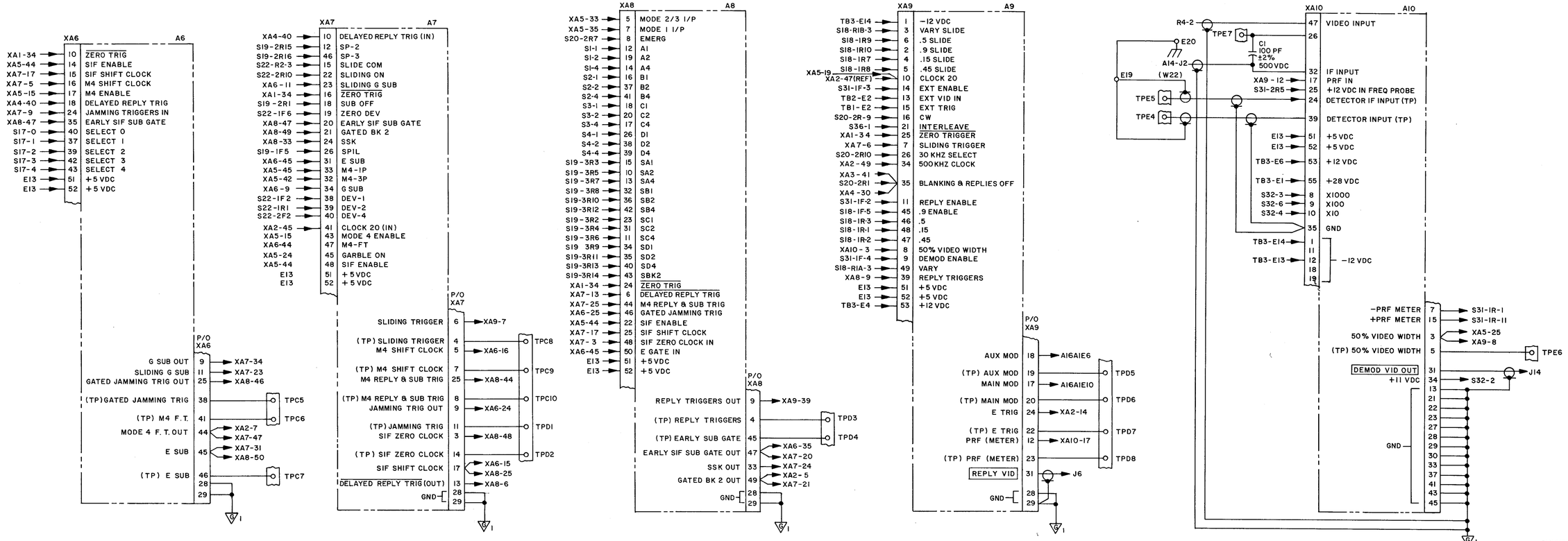


Figure FO-19. Test set, schematic diagram (sheet 6 of 6).

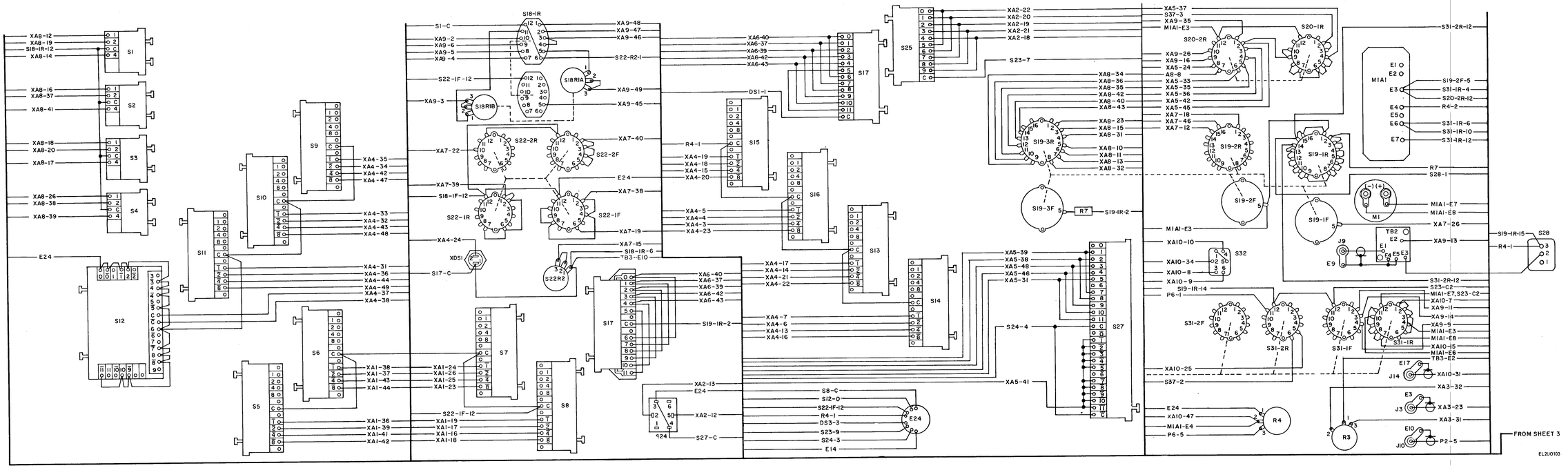


Figure FO-20. Test set, wiring diagram (sheet 1 of 4).

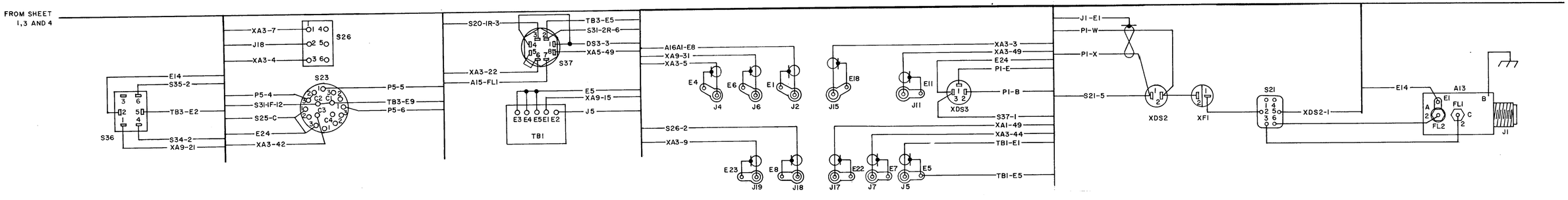
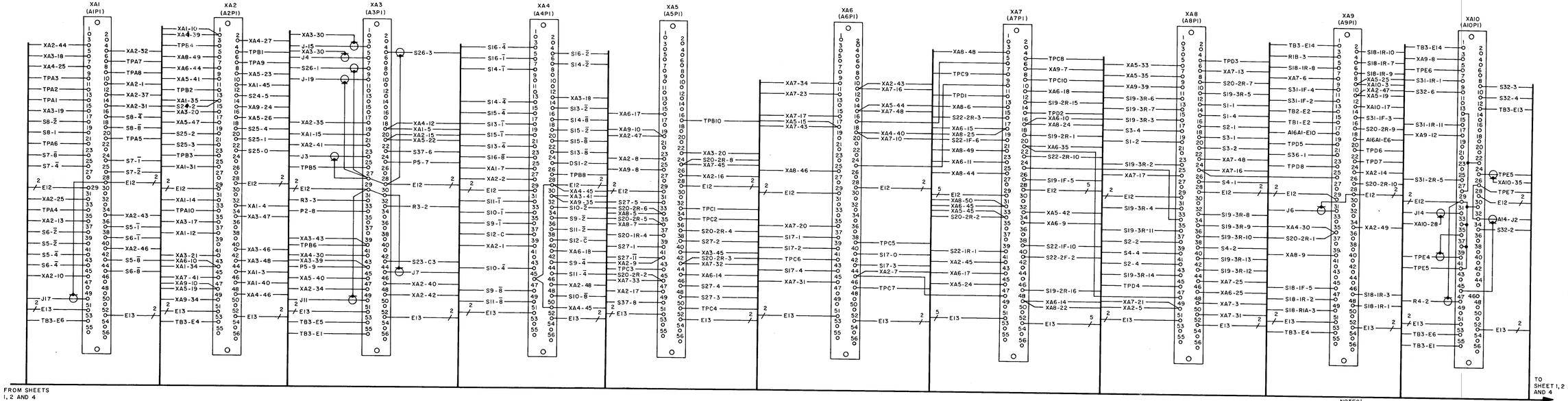


Figure FO–20. Test set, wiring diagram (sheet 2 of 4).

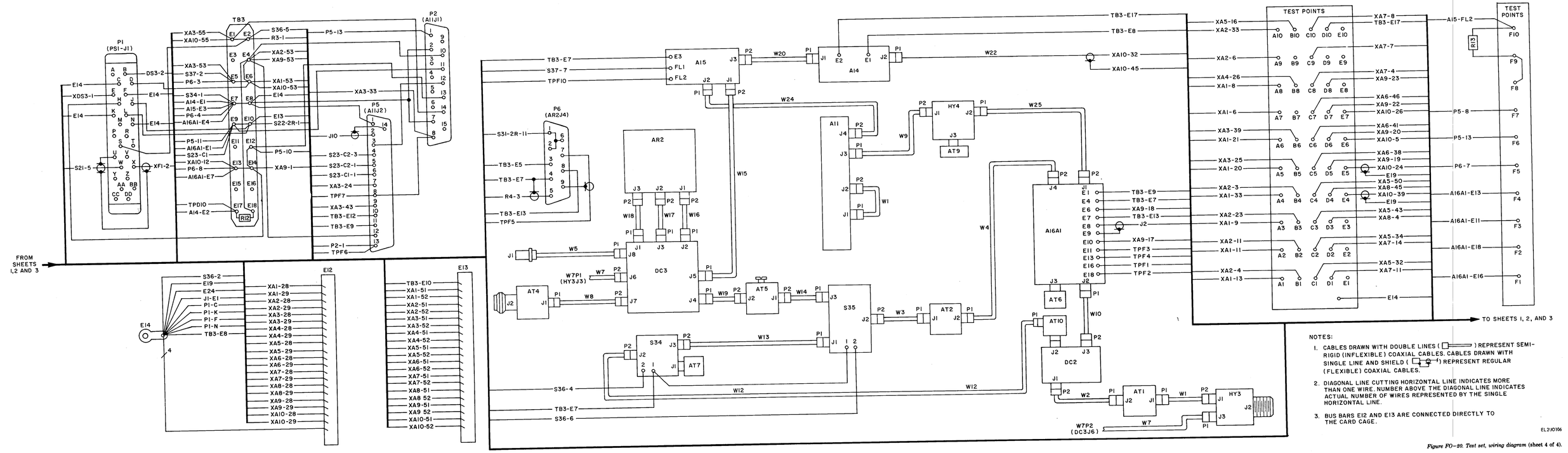


NOTES:

1. DIAGONAL LINE CUTTING HORIZONTAL LINE INDICATES MORE THAN ONE WIRE NUMBER ABOVE THE DIAGONAL LINE INDICATES ACTUAL NUMBER OF WIRES REPRESENTED BY THE SINGLE HORIZONTAL LINE.

EL2U0105

Figure FO-20. Test set, wiring diagram (sheet 3 of 4).

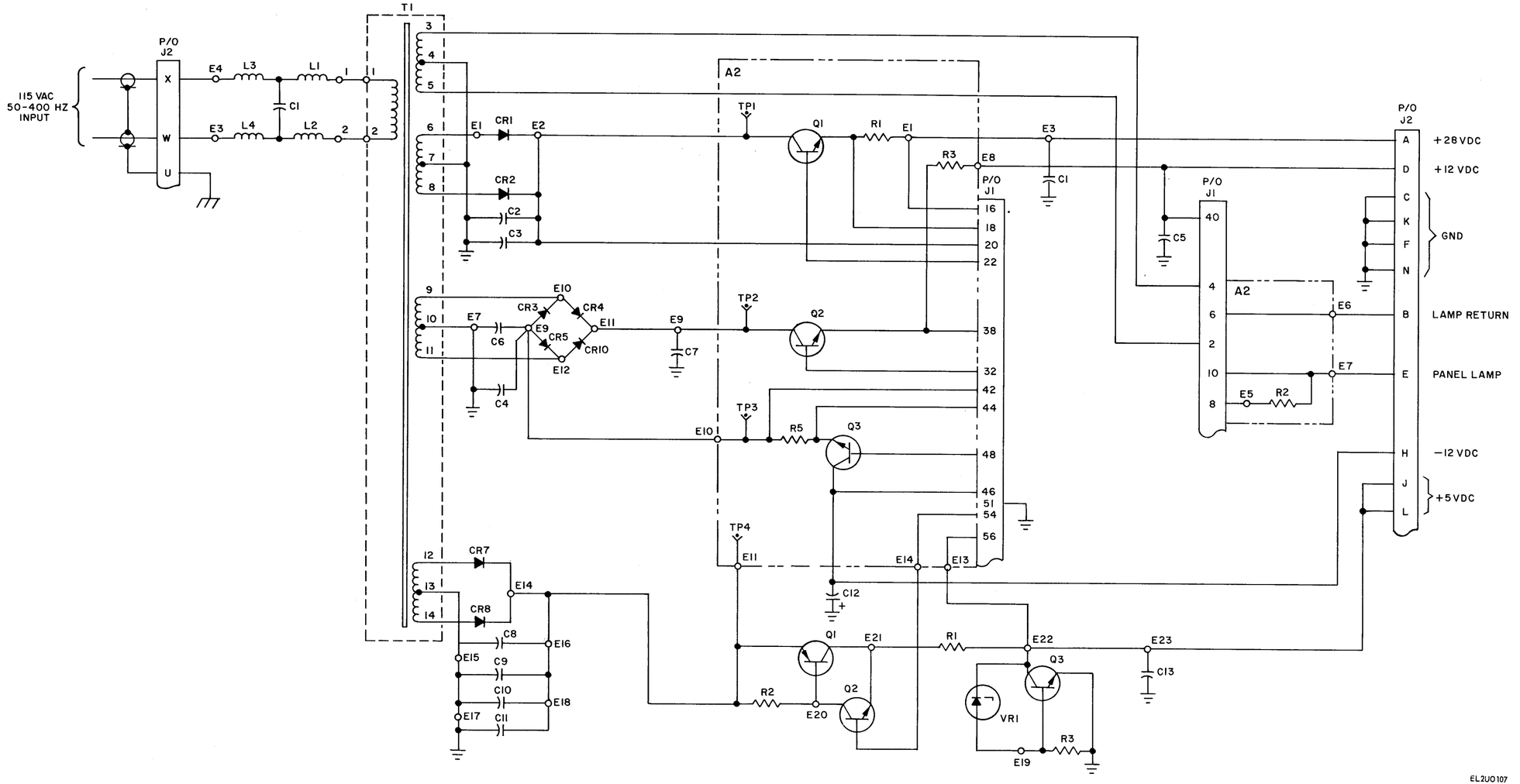


NOTES:

1. CABLES DRAWN WITH DOUBLE LINES ( ) REPRESENT SEMI-RIGID (INFLEXIBLE) COAXIAL CABLES. CABLES DRAWN WITH SINGLE LINE AND SHIELD ( ) REPRESENT REGULAR (FLEXIBLE) COAXIAL CABLES.
2. DIAGONAL LINE CUTTING HORIZONTAL LINE INDICATES MORE THAN ONE WIRE. NUMBER ABOVE THE DIAGONAL LINE INDICATES ACTUAL NUMBER OF WIRES REPRESENTED BY THE SINGLE HORIZONTAL LINE.
3. BUS BARS E12 AND E13 ARE CONNECTED DIRECTLY TO THE CARD CAGE.

EL2J0106

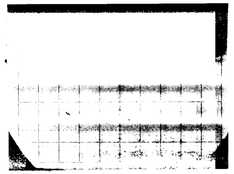
Figure FO-20. Test set, wiring diagram (sheet 4 of 4).



EL2UO107

Figure FO-21. Power supply, schematic diagram

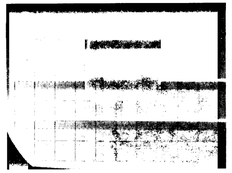
TEST POINT (A INPUT) TPA2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .2 MSEC
DELAYED TIME/DIV: 50 μSEC

TEST SET
SEE TABLE 3-1

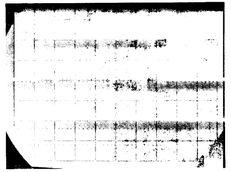
TEST POINT (A INPUT) TPA3-1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .2 MSEC
DELAYED TIME/DIV: 20 μSEC

TEST SET
SEE TABLE 3-1

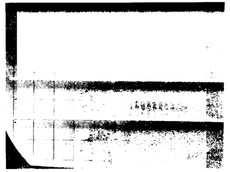
TEST POINT (A INPUT) TPA3-2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .2 MSEC
DELAYED TIME/DIV: 20 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P

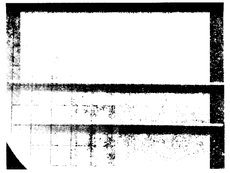
TEST POINT (A INPUT) TPA4



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .2 MSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1

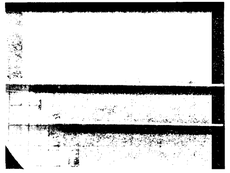
TEST POINT (A INPUT) TPA5



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .2 MSEC
DELAYED TIME/DIV: 20 μSEC

TEST SET
SEE TABLE 3-1

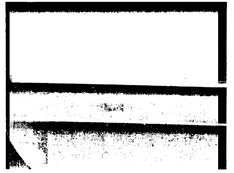
TEST POINT (A INPUT) TPA6



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .2 MSEC
DELAYED TIME/DIV: 20 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P

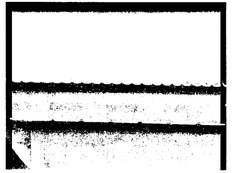
TEST POINT (A INPUT) TPA7-1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .2 MSEC
DELAYED TIME/DIV: 20 μSEC

TEST SET
SEE TABLE 3-1

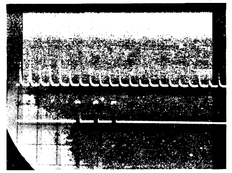
TEST POINT (A INPUT) TPA7-2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .2 MSEC
DELAYED TIME/DIV: 2 μSEC

TEST SET
SEE TABLE 3-1

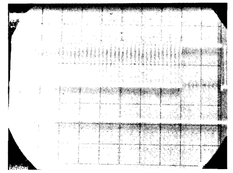
TEST POINT (A INPUT) TPA8



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .2 MSEC
DELAYED TIME/DIV: 2 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P

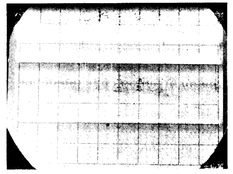
TEST POINT (A INPUT) TPA9



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 50 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P

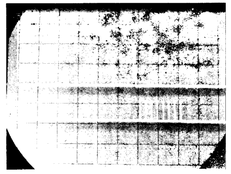
TEST POINT (A INPUT) TPA10



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 50 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P

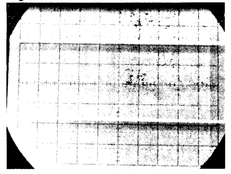
TEST POINT (A INPUT) TPB1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1

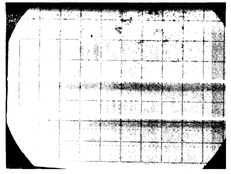
TEST POINT (A INPUT) TPB2



OSCILLOSCOPE
A VOLTS/DIV: 2 (0 VDC AT CENTER GRATICULE)
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1

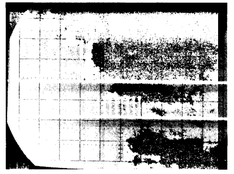
TEST POINT (A INPUT) TPB3-1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
SIF CHAL VID SIF MODE SEL: 1

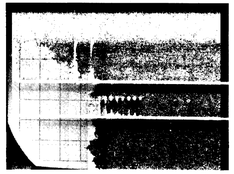
TEST POINT (B INPUT) TPB3-2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
SIF CHAL VID SIF MODE SEL: 2

TEST POINT (B INPUT) TPB3-3



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
SIF CHAL VID SIF MODE SEL: 3/A

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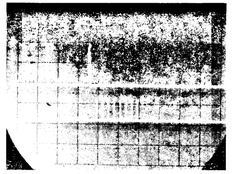
Figure FO-22. Waveform diagram (Sheet 1 of 4).

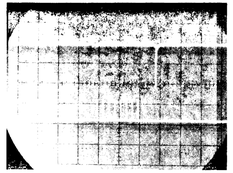
TEST POINT (B INPUT) TPB3-4



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
SIF CHAL VID SIF MODE SEL: C

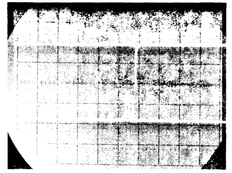
TEST POINT (B INPUT) TPB4-1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1

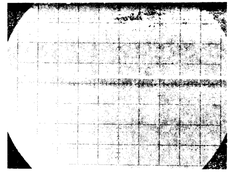
TEST POINT (A INPUT) TPB4-2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P

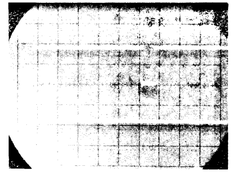
TEST POINT (A INPUT) TPB5



OSCILLOSCOPE
A VOLTS/DIV: .5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .5 μSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1 EXCEPT:
SIG GEN FUNCTION: SWP ±15 MHZ OR SWP ±5 MHZ

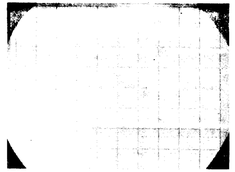
TEST POINT (A INPUT) TPB6-1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 2 MSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1 EXCEPT:
SIG GEN FUNCTION SEL: SWP ±5 MHZ

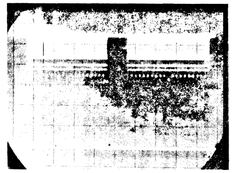
TEST POINT (A INPUT) TPB6-2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 2 MSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1 EXCEPT:
SIG GEN FUNCTION SEL: SWP ±15 MHZ

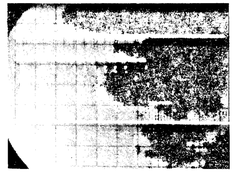
TEST POINT (A INPUT) TPB8-1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .5 MSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES RANGE DELAY SEL: 1999
PRT SEL (USEC): 2500

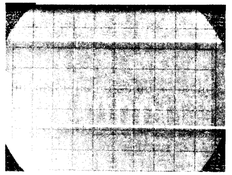
TEST POINT (A INPUT) TPB8-2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .5 MSEC
DELAYED TIME/DIV: 20 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES RANGE DEL SEL: 1111
PRT SEL (USEC): 2500

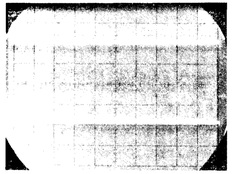
TEST POINT (A INPUT) TPB8-3



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .5 MSEC
DELAYED TIME/DIV: 50 μSEC

TEST SET
SEE TABLE 3-1

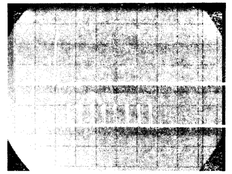
TEST POINT (A INPUT) TPB10



OSCILLOSCOPE
A VOLTS/DIV: 2 (0 VDC AT CENTER GRATICULE)
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P

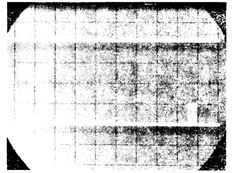
TEST POINT (A INPUT) TPC1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 5 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
SIF CHAL VID SIF MODE SEL: 1
TRIG SEL DCD MODE SEL: 1
BIT (MOM): PRESSED

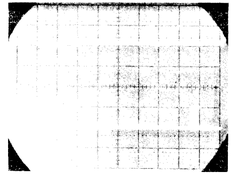
TEST POINT (A INPUT) TPC2



OSCILLOSCOPE
A VOLTS/DIV: 2 (0 VDC AT CENTER GRATICULE)
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1

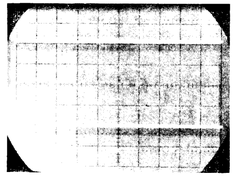
TEST POINT (A INPUT) TPC3



OSCILLOSCOPE
A VOLTS/DIV: 2 (0 VDC AT CENTER GRATICULE)
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1

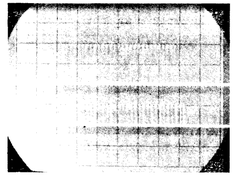
TEST POINT (A INPUT) TPC4



OSCILLOSCOPE
A VOLTS/DIV: 2 (0 VDC AT CENTER GRATICULE)
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P

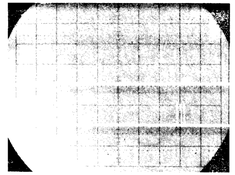
TEST POINT (A INPUT) TPC5-1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P
M4 JAMMING: 5

TEST POINT (A INPUT) TPC5-2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P
M4 JAMMING: 1

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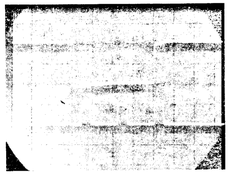
Figure FO-22. Waveform diagram (Sheet 2 of 4).

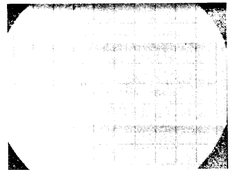
TEST POINT (A INPUT) TPC6



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: 1 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P

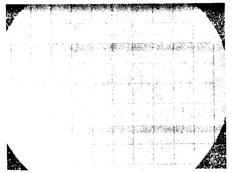
TEST POINT (A INPUT) TPC7-1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: 5 μSEC

TEST SET
SEE TABLE 3-3 EXCEPT:
REPLIES SUB PULSE SEL: A1

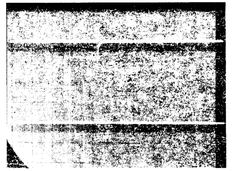
TEST POINT (A INPUT) TPC7-2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P

TEST POINT (A INPUT) TPC8-1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: 10 μSEC

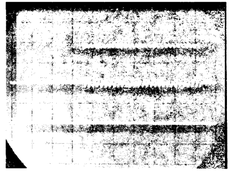
TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES
SUB PULSE POS SELECT: VARY
SUB PULSE POS VARY: FULLY CCW
SUB PULSE SEL: A1

TEST POINT (A INPUT) TPC8-2

OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: 2 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P
SUB PULSE POS SELECT: VARY
SUB PULSE POS VARY: FULLY CCW
SUB PULSE SEL: M4-P2

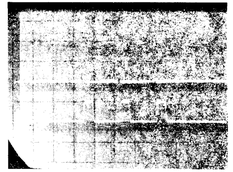
TEST POINT (A INPUT) TPC9



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: 20 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P

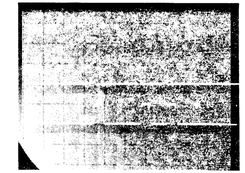
TEST POINT (A INPUT) TPC10-1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: 1 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P

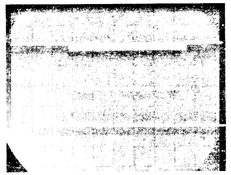
TEST POINT (A INPUT) TPC10-2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: 1 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-3P
SUB PULSE POS SELECT: +.50
SUB PULSE SEL: M4-P2

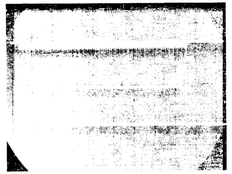
TEST POINT (A INPUT) TPD1-1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 20 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: EMERG
PRT SEL (USEC): 0550

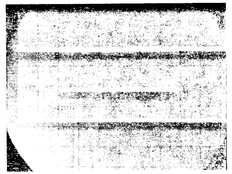
TEST POINT (A INPUT) TPD1-2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 20 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES MODULATION SEL: M4-P3
M4 JAMMING: 5

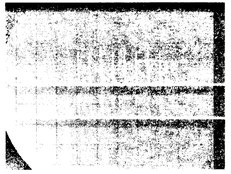
TEST POINT (A INPUT) TPD2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 20 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
PRT SEL (USEC): 0550

TEST POINT (A INPUT) TPD3



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 5 μSEC

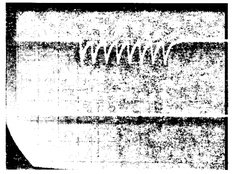
TEST SET
SEE TABLE 3-1

TEST POINT (A INPUT) TPD4

OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 5 μSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
REPLIES SUB PULSE SEL: A1

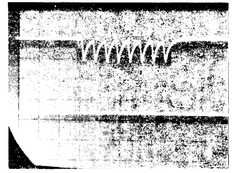
TEST POINT (A INPUT) TPD5



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 5 μSEC

TEST SET
SEE TABLE 3-1

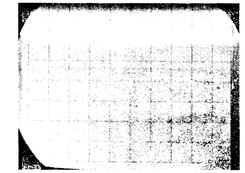
TEST POINT (A INPUT) TPD6



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 5 μSEC

TEST SET
SEE TABLE 3-1

TEST POINT (A INPUT) TPD7-1



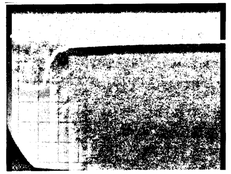
OSCILLOSCOPE
A VOLTS/DIV: 2
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1 EXCEPT:
TRIG SEL INT/DCD/EXT: EXT (TRIGGER FROM EXTERNAL PULSE GENERATOR AT 2000 HZ)

EL2UO110

Figure FO-22. Waveform diagram (Sheet 3 of 4).

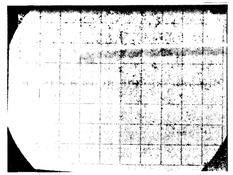
TEST POINT (A INPUT) TPD7-2



OSCILLOSCOPE
A VOLTS/DIV: 2
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 μSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1 EXCEPT:
TRIG SEL INT/DCD/EXT: EXT (TRIGGER FROM EXTERNAL PULSE GENERATOR AT 2000 HZ)

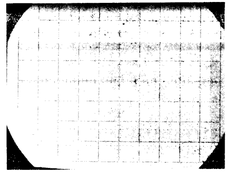
TEST POINT (A INPUT) TPD8



OSCILLOSCOPE
A VOLTS/DIV: 2
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 μSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1

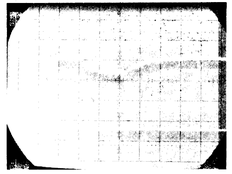
TEST POINT (A INPUT) TPD10



OSCILLOSCOPE
A VOLTS/DIV: 5 (0 VDC AT CENTER OF GRATICULE
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: 50 μSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1

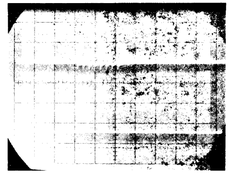
TEST POINT (A INPUT) TPE4



OSCILLOSCOPE
A VOLTS/DIV: .2
A AC/GND/DC: AC
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1 (SUM RF IN/OUT CONNECTED TO LOW PWR IN)

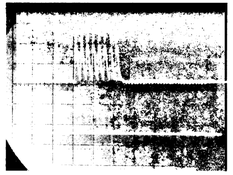
TEST POINT (A INPUT) TPE5



OSCILLOSCOPE
A VOLTS/DIV: .2
A AC/GND/DC: AC
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1 (SUM RF IN/OUT CONNECTED TO LOW PWR IN)

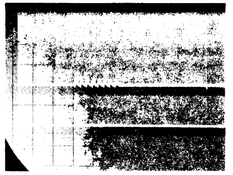
TEST POINT (A INPUT) TPE6



OSCILLOSCOPE
A VOLTS/DIV: 1
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1 (SUM RF IN/OUT CONNECTED TO LOW PWR IN)

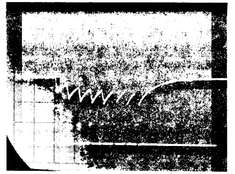
TEST POINT (A INPUT) TPE7



OSCILLOSCOPE
A VOLTS/DIV: .02
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 10 μSEC

TEST SET
SEE TABLE 3-1 (SUM RF IN/OUT CONNECTED TO LOW PWR IN)

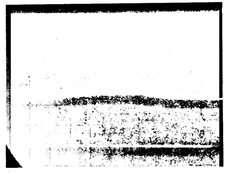
TEST POINT (A INPUT) TPF1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 5 μSEC

TEST SET
SEE TABLE 3-1

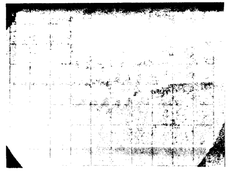
TEST POINT (A INPUT) TPF2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 5 μSEC

TEST SET
SEE TABLE 3-1

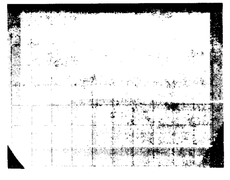
TEST POINT (A INPUT) TPF3



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 5 μSEC

TEST SET
SEE TABLE 3-1

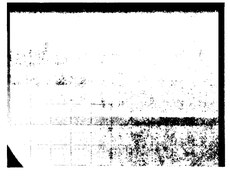
TEST POINT (A INPUT) TPF4



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: 5 μSEC

TEST SET
SEE TABLE 3-1

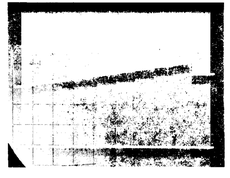
TEST POINT (A INPUT) TPF5



OSCILLOSCOPE
A VOLTS/DIV: 5 (0 VDC AT CENTER GRATICULE)
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1

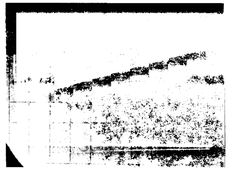
TEST POINT (A INPUT) TPF6-1



OSCILLOSCOPE
A VOLTS/DIV: 1
B VOLTS/DIV: 5 (FREQ MKRS OUT)
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1 EXCEPT:
SIG GEN FUNCTION: SWP ±5 MHZ

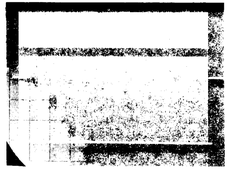
TEST POINT (A INPUT) TPF6-2



OSCILLOSCOPE
A VOLTS/DIV: 1
B VOLTS/DIV: 5 (FREQ MKRS OUT)
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .1 MSEC
DELAYED TIME/DIV: OFF
SWEEP DISPLAY: MAIN

TEST SET
SEE TABLE 3-1 EXCEPT:
SIG GEN FUNCTION: SWP 15 MHZ

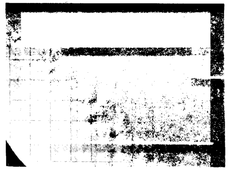
TEST POINT (A INPUT) TPF7-1



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5 (FREQ MKRS OUT)
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .5 MSEC
DELAYED TIME/DIV: .1 MSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
SIG GEN FUNCTION: SWP ±5 MHZ

TEST POINT (A INPUT) TPF8-2



OSCILLOSCOPE
A VOLTS/DIV: 2
B VOLTS/DIV: 5 (FREQ MKRS OUT)
EXT÷10/EXT/INT/LINE: EXT (SCOPE TRIG OUT)
MAIN TIME/DIV: .5 MSEC
DELAYED TIME/DIV: .2 MSEC

TEST SET
SEE TABLE 3-1 EXCEPT:
SIG GEN FUNCTION: SWP ±15 MHZ

EL2U0111

Figure FO-22. Waveform diagram (Sheet 4 of 4).

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